

NEC

DATA SHEET

MOS INTEGRATED CIRCUIT μ PD78P356(A)

16 BIT SINGLE-CHIP MICROCOMPUTER

The μ PD78P356(A) is produced by replacing the internal mask ROM of the μ PD78356(A) with a one-time PROM. One-time PROM products, in which data can be written once are effective for manufacture of small quantities of multiple products and early stage start-up of application.

The following user's manuals completely describe the functions of the μ PD78P356(A). Be sure to read them before designing an application system.

μ PD78356 User's Manual, Hardware : U10669E

μ PD78356 User's Manual, Instruction : IEU-1395

FEATURES

- Higher reliability relative to the μ PD78P356
- Compatible with the μ PD78356(A)
 - Can be replaced with the μ PD78356(A) containing mask ROM on a full-production basis.
- Internal PROM: 48K bytes
 - Data can be written once
- Contained ECC circuit
 - The circuit ensures that highly reliable data is stored in the internal PROM.
- PROM programming: Same as for the μ PD27C1001A
- QTOP™ microcomputer

Remark The QTOP microcomputer is a single-chip microcomputer with a built-in one-time PROM that is totally supported by NEC. The support includes writing application programs, marking, screening, and verification.

ORDERING INFORMATION

Part number	Package	Internal ROM
μ PD78P356GD(A)-5BB	120-pin plastic QFP (28 × 28 mm)	One-time PROM

QUALITY GRADE

Special

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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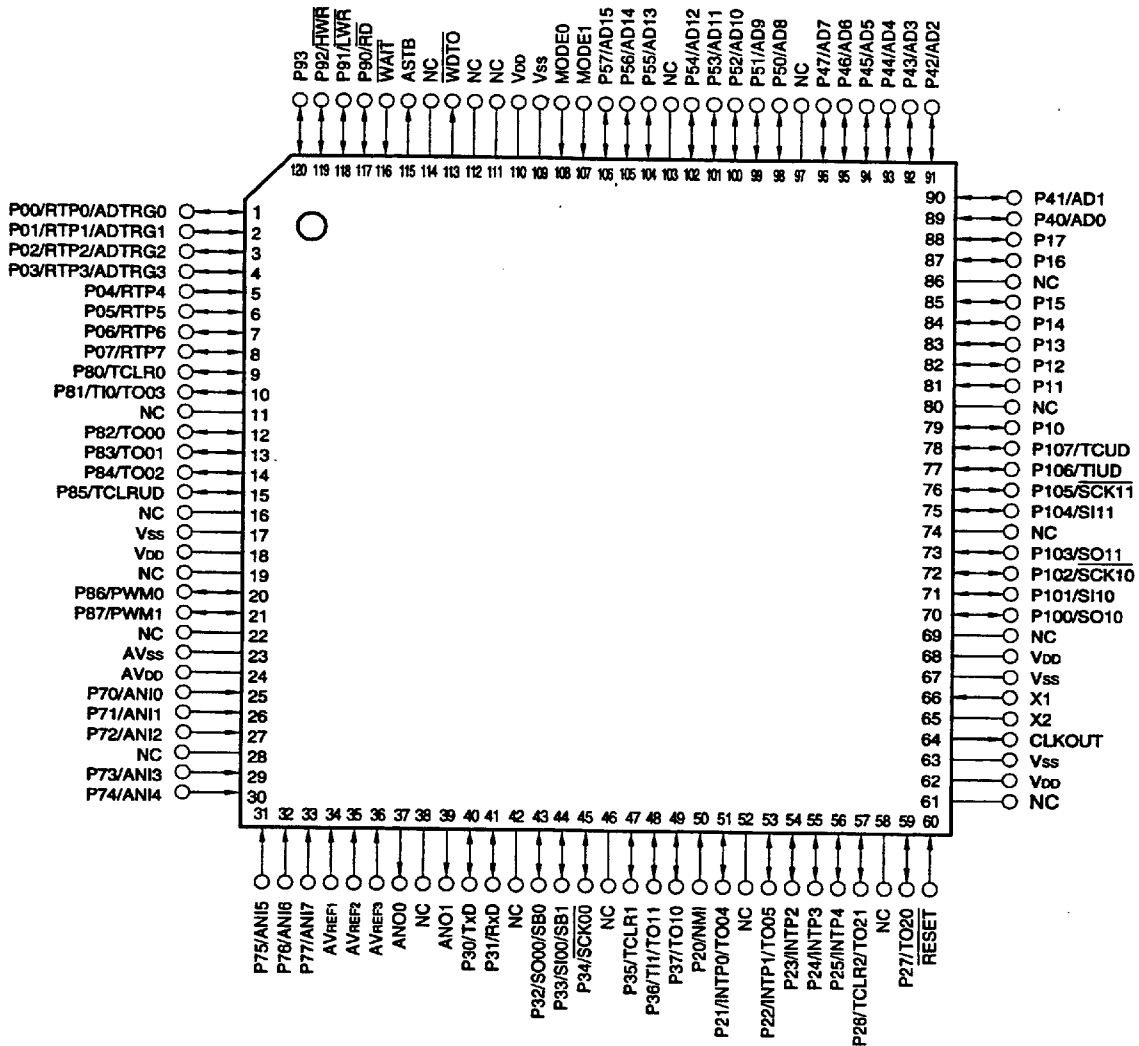
DIFFERENCES BETWEEN THE μPD78P356 AND μPD78P356(A)

Item \ Product	μPD78P356	μPD78P356(A)
Quality grade	Standard	Special
Operating ambient temperature (TA)	-10 to +70 °C	-40 to +85 °C
Operating frequency	8 to 32 MHz	8 to 25 MHz
Minimum instruction execution time	125 ns (external clock: 32 MHz)	160 ns (external clock: 25 MHz)
Allowable pin injection current when overvoltage is applied	Not allowed	Specified
DC characteristics	Differ in their V _{DD} supply currents and data hold currents.	
AC characteristics	Differ in their bus timings.	
A/D converter characteristics	Differ in their sampling times.	
Package	100-pin plastic QFP (14 × 14 mm) 120-pin plastic QFP (28 × 28 mm) 120-pin ceramic WQFN	120-pin plastic QFP (28 × 28 mm)

PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode (MODE0 = L, MODE1 = L)

- 120-pin plastic QFP (28 × 28 mm)
μPD78P356GD(A)-5BB



Caution Connect the MODE0 and MODE1 pins directly to the Vss pins.

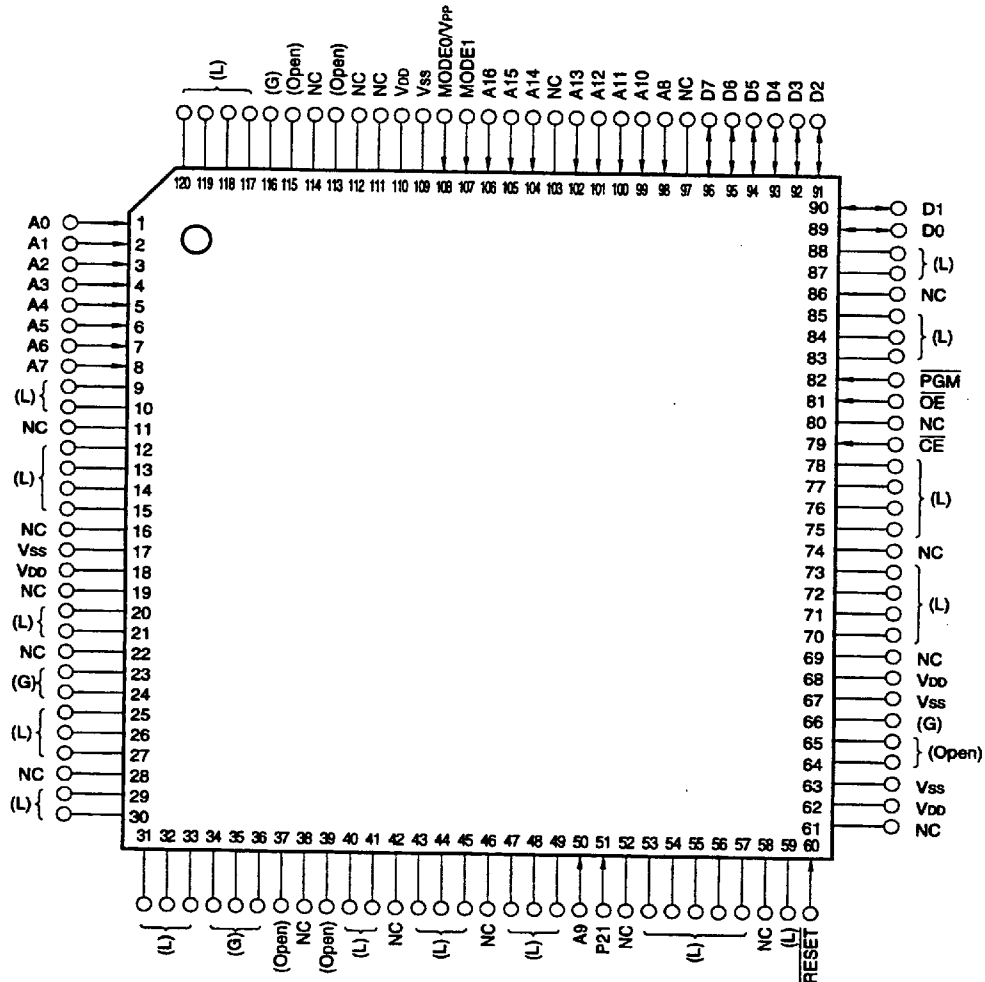
Remark Pin compatible with the μPD78356GD(A)

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P00-P07	: Port 0	SI00, SI10	: } Serial input
P10-P17	: Port 1	SI11	: }
P20-P27	: Port 2	SO00, SO10	: } Serial output
P30-P37	: Port 3	SO11	: }
P40-P47	: Port 4	SB0, SB1	: Serial bus
P50-P57	: Port 5	$\overline{SCK00}$, $\overline{SCK10}$: } Serial clock
P70-P77	: Port 7	$\overline{SCK11}$: }
P80-P87	: Port 8	PWM0, PWM1	: Pulse width modulation output
P90-P93	: Port 9	\overline{WDTO}	: Watchdog timer output
P100-P107	: Port 10	MODE0, MODE1	: Mode
RTP0-RTP7	: Real-time port	AD0-AD15	: Address/data bus
NMI	: Nonmaskable interrupt	ASTB	: Address strobe
INTP0-INTP4	: Interrupt from peripherals	\overline{RD}	: Read strobe
TO00-TO05	: } Timer output	\overline{LWR}	: Low-address write strobe
TO10, TO11	: }	\overline{HWR}	: High-address write strobe
TO20, TO21	: }	\overline{WAIT}	: Wait
TCLR0-TCLR2	: } Timer clear input	CLKOUT	: Clock output
TCLRUD	: }	\overline{RESET}	: Reset
TI0, TI1	: Timer input	X1, X2	: Crystal
TIUD	: Count pulse input	AV _{DD}	: Analog V _{DD}
TCUD	: Control pulse input	AV _{SS}	: Analog V _{SS}
ANI0-ANI7	: Analog input	AV _{REF1} -AV _{REF3}	: Analog reference voltage
ADTRG0-ADTRG3	: A/D trigger input	V _{DD}	: Power supply
ANO0, ANO1	: Analog output	V _{SS}	: Ground
TxD	: Transmit data	NC	: No connection
RxD	: Receive data		

(2) PROM programming mode (MODE0/V_{PP} = +5 V, MODE1 = G, P21 = G, $\overline{\text{RESET}}$ = G)

- 120-pin plastic QFP (28 × 28 mm)
μPD78P356GD(A)-5BB



Caution Symbols in parentheses denote how the pins not used in the PROM programming mode should be treated.

L : Connect these pins to the V_{ss} pins through separate resistors.

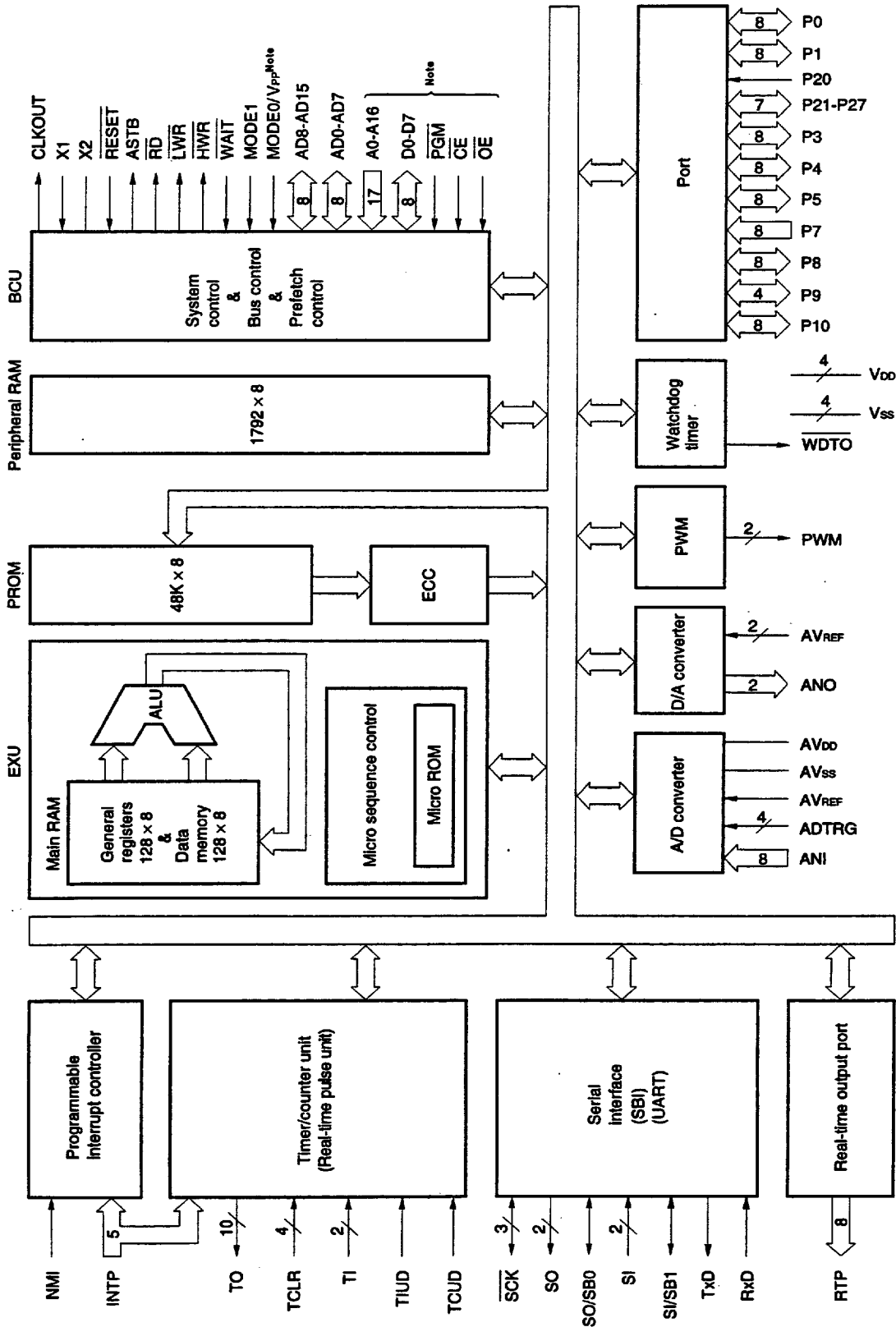
G : Connect these pins to the V_{ss} pins.

Open: Do not connect these pins to anything.

A0-A16 :	Address bus	MODE0, MODE1 :	} Programming mode set
D0-D7 :	Data bus	P21	
$\overline{\text{CE}}$:	Chip enable	$\overline{\text{RESET}}$	
$\overline{\text{OE}}$:	Output enable	V _{DD} :	Power supply
PGM :	Programming mode	V _{SS} :	Ground
		V _{PP} :	Programming power supply

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BLOCK DIAGRAM



Note Pins used in the PROM programming mode

CONTENTS

1. PIN FUNCTIONS	8
1.1 NORMAL OPERATION MODE (MODE0 = L, MODE1 = L)	8
1.2 PROM PROGRAMMING MODE (MODE0/V_{PP} = H, MODE1 = L, P21 = L, $\overline{\text{RESET}}$ = L)	12
1.3 INPUT/OUTPUT CIRCUIT TYPE FOR EACH PIN AND HANDLING OF UNUSED PINS	13
2. DIFFERENCES BETWEEN THE μPD78P356(A) AND μPD78356(A)	16
3. PROM PROGRAMMING	17
3.1 OPERATION MODE	18
3.2 PROCEDURE FOR WRITING ON PROM (PAGE PROGRAM MODE)	19
3.3 PROCEDURE FOR WRITING ON PROM (BYTE PROGRAM MODE)	21
3.4 PROCEDURE FOR READING FROM PROM	24
4. SCREENING ONE-TIME PROM PRODUCTS	25
5. ELECTRICAL CHARACTERISTICS	26
6. CHARACTERISTIC CURVES (FOR REFERENCE)	49
7. PACKAGE DRAWINGS	52
8. RECOMMENDED SOLDERING CONDITIONS	53
APPENDIX A TOOLS	54
A.1 DEVELOPMENT TOOLS	54
A.2 EMBEDDED SOFTWARE	59
APPENDIX B DRAWINGS OF THE CONVERSION SOCKET AND RECOMMENDED PATTERN ON BOARDS	61

1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE (MODE0 = L, MODE1 = L)

(1) Port pins (1/2)

Pin	I/O	Function	Dual-function pin
P00	I/O	Port 0. 8-bit I/O port. Can be specified as input or output bit by bit.	RTP0/ADTRG0
P01			RTP1/ADTRG1
P02			RTP2/ADTRG2
P03			RTP3/ADTRG3
P04-P07			RTP4-RTP7
P10-P17	I/O	Port 1. 8-bit I/O port. Can be specified as input or output bit by bit.	-
P20	I	Port 2. 8-bit I/O port. Can be specified as input or output bit by bit. (P20/NMI is excluded.)	NMI
P21	I/O		INTP0/TO04
P22			INTP1/TO05
P23			INTP2
P24			INTP3
P25			INTP4
P26			TCLR2/TO21
P27			TO20
P30	I/O	Port 3. 8-bit I/O port. Can be specified as input or output bit by bit.	TxD
P31			RxD
P32			SO00/SB0
P33			SI00/SB1
P34			SCK00
P35			TCLR1
P36			TI1/TO11
P37			TO10
P40-P47	I/O	Port 4. 8-bit I/O port. Can be specified as input or output in units of 8 bits.	AD0-AD7
P50-P57	I/O	Port 5. 8-bit I/O port. Can be specified as input or output bit by bit.	AD8-AD15
P70-P77	I	Port 7. Port used only for 8-bit input.	ANI0-ANI7

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(1) Port pins (2/2)

Pin	I/O	Function	Dual-function pin
P80	I/O	Port 8. 8-bit I/O port. Can be specified as input or output bit by bit.	TCLR0
P81			TI0/TO03
P82			TO00
P83			TO01
P84			TO02
P85			TCLRUD
P86			PWM0
P87			PWM1
P90	I/O	Port 9. 4-bit I/O port. Can be specified as input or output bit by bit.	\overline{RD}
P91			\overline{LWR}
P92			HWR
P93			-
P100	I/O	Port 10. 8-bit I/O port. Can be specified as input or output bit by bit.	SO10
P101			SI10
P102			$\overline{SCK10}$
P103			SO11
P104			SI11
P105			$\overline{SCK11}$
P106			TIUD
P107			TCUD

(2) Non-port pins (1/3)

Pin	I/O	Function	Dual-function pin
RTP0	O	Outputs a pulse in real time as triggered by a trigger signal sent from the real-time pulse unit.	P00/ADTRG0
RTP1			P01/ADTRG1
RTP2			P02/ADTRG2
RTP3			P03/ADTRG3
RTP4-RTP7			P04-P07
NMI	I	Nonmaskable interrupt request input	P20
INTP0		External interrupt request input	P21/TO04
INTP1			P22/TO05
INTP2			P23
INTP3			P24
INTP4	P25		
TI0	I	External count clock input to timer 0	P81/TO03
TI1		External count clock input to timer 1	P36/TO11
TIUD		External count clock input to the up/down counter	P106
TCUD		Input for the control signal to determine whether the up/down counter counts up or down.	P107
TCLR0		Clear signal input to the real-time pulse unit	P80
TCLR1			P35
TCLR2			P26/TO21
TCLRUD			P85
TO00	O	Timer output from the real-time pulse unit (RPU)	P82
TO01			P83
TO02			P84
TO03			P81/TI0
TO04			P21/INTP0
TO05			P22/INTP1
TO10			P37
TO11			P36/TI1
TO20			P27
TO21			P26/TCLR2
ANI0-ANI7			I
ADTRG0	External trigger signal input to the A/D converter	P00/RTP0	
ADTRG1		P01/RTP1	
ADTRG2		P02/RTP2	
ADTRG3	P03/RTP3		
ANO0	O	Analog output from the D/A converter	-
ANO1			-
TxD	O	Serial data output from the asynchronous serial interface	P30
RxD	I	Serial data input to the asynchronous serial interface	P31

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(2) Non-port pins (2/3)

Pin	I/O	Function	Dual-function pin
SCK00	I/O	Serial clock I/O for the clock synchronous serial interface	P34
SCK10			P102
SCK11			P105
SI00	I	Serial data input to the clock synchronous serial interface in the 3-wire mode	P33/SB1
SI10			P101
SI11			P104
SO00	O	Serial data output from the clock synchronous serial interface in the 3-wire mode	P32/SB0
SO10			P100
SO11			P103
SB0	I/O	Serial data I/O for the clock synchronous serial interface in the SBI mode	P32/SO00
SB1			P33/SI00
PWM0	O	PWM signal output	P86
PWM1			P87
WDTO	O	Output for the signal which indicates the watchdog timer overflowed. (A nonmaskable interrupt is generated.)	—
AD0-AD7	I/O	Eight low-order bits of multiplexed address/data bus, used when external memory is expanded	P40-P47
AD8-AD15		<ul style="list-style-type: none"> When external 8-bit bus is specified Eight high-order bits of address bus, used when external memory is expanded. The number of pins used as the address bus varies with the external address space. When external 16-bit bus is specified Eight high-order bits of multiplexed address/data bus, used when external memory is expanded 	P50-P57
ASTB	O	Output for the timing signal used in externally latching address information output from the AD0 to AD15 pins, in order to access the external memory	—
RD		Read strobe signal output to the external memory	P90
LWR		<ul style="list-style-type: none"> When external 8-bit bus is specified Write strobe signal output to external memory When external 16-bit bus is specified Write strobe signal output to the eight low-order bits of external memory 	P91
HWR		<ul style="list-style-type: none"> When external 8-bit bus is specified General-purpose port When external 16-bit bus is specified Write strobe signal output to the eight high-order bits of external memory 	P92
WAIT	I	Input for the control signal which causes wait in the bus cycle	—
MODE0	I	Input for the control signal which sets the operation mode. Normally, both MODE0 and MODE1 are directly connected to the Vss pin.	—
MODE1			—
CLKOUT	O	System clock output	—
RESET	I	System reset input	—
X1	I	Crystal input pin for the system clock. A clock signal provided externally is input to the X1 pin. The X2 pin is left open.	—
X2	—		—

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(2) Non-port pins (3/3)

Pin	I/O	Function	Dual-function pin
AVREF1	I	A/D converter reference voltage input	-
AVREF2		D/A converter reference voltage input	-
AVREF3			-
AVDD	-	Analog power supply for the A/D converter	-
AVSS	-	Ground for the A/D converter	-
VDD	-	Positive power supply	-
VSS	-	Ground	-
NC	-	Not internally connected. Connect the NC pin to the VSS pin (can also be left open).	-

1.2 PROM PROGRAMMING MODE (MODE0/VPP = H, MODE1 = L, P21 = L, $\overline{\text{RESET}}$ = L)

Pin	I/O	Function
MODE0/VPP	I	PROM programming mode set/programming supply voltage
MODE1	I	PROM programming mode set
P21		
$\overline{\text{RESET}}$		
A0-A16	I	Address bus
D0-D7	I/O	Data bus
PGM	I	Program input
$\overline{\text{CE}}$	I	Enable PROM
$\overline{\text{OE}}$	I	Read strobe to PROM
VDD	-	Positive power supply
VSS		GND

Caution Connect the MODE0/VPP, MODE1, P21, and $\overline{\text{RESET}}$ pins directly to the VDD or VSS pin.

1.3 INPUT/OUTPUT CIRCUIT TYPE FOR EACH PIN AND HANDLING OF UNUSED PINS

Table 1-1 lists the input and output circuit type for each pin and how to handle it when it is not used. Fig. 1-1 shows the circuits.

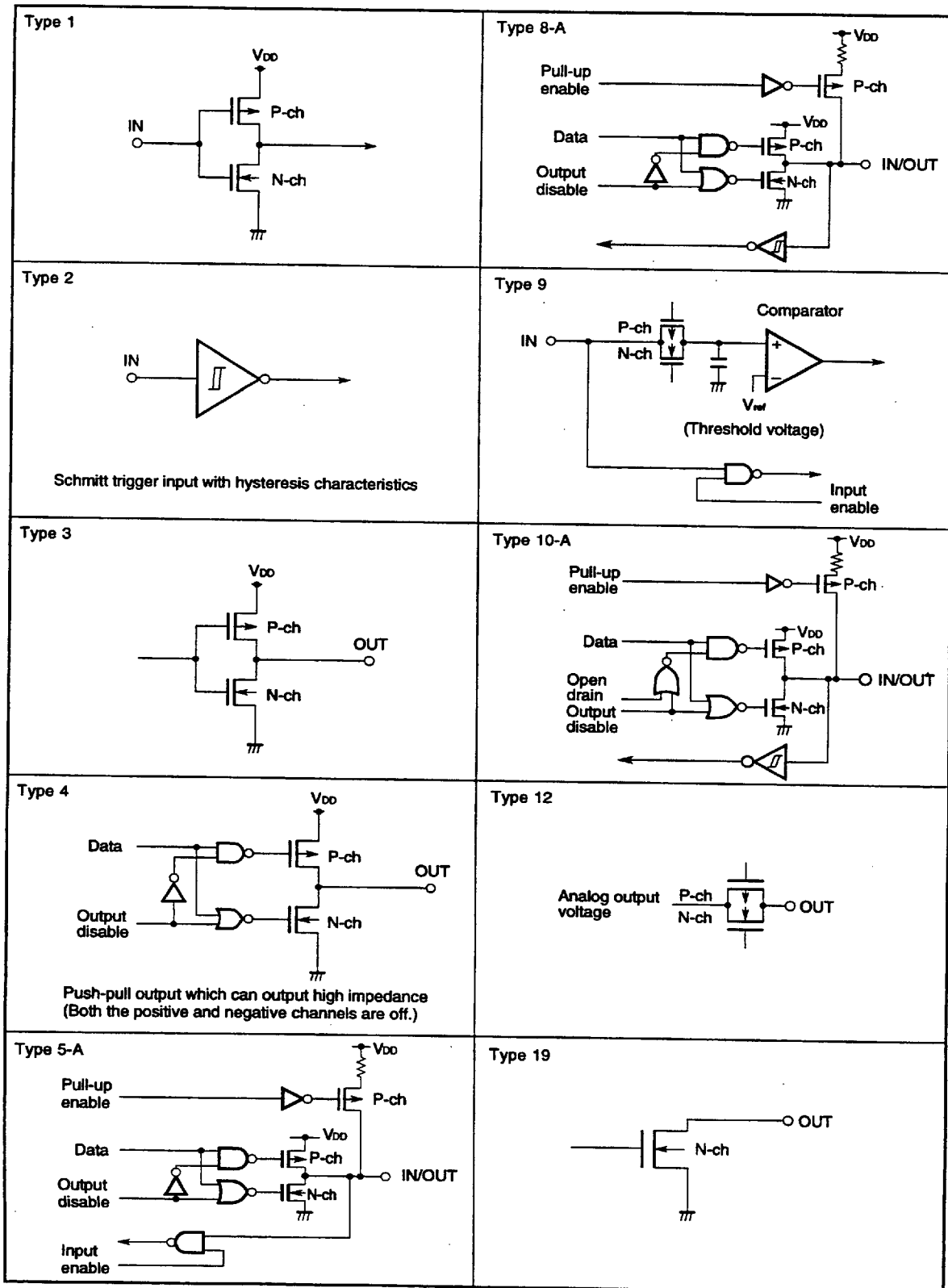
Table 1-1 Input/Output Circuit Type for Each Pin and Recommended Connection Methods for Unused Pins (1/2)

Pin	I/O circuit type	Recommended connection method
P00/RTP0/ADTRG0-P03/RTP3/ADTRG3	8-A	Input state : Each pin is connected to the V _{DD} or V _{SS} pin via a separate resistor. Output state : Open
P04/RTP4-P07/RTP7	5-A	
P10-P17		
P20/NMI	2	Connected to the V _{SS} pin.
P21/INTP0/TO04	8-A	Input state : Each pin is connected to the V _{DD} or V _{SS} pin via a separate resistor. Output state : Open
P22/INTP1/TO05		
P23/INTP2		
P24/INTP3		
P25/INTP4		
P26/TCLR2/TO21		
P27/TO20		
P30/TxD		
P31/RxD		
P32/SO00/SB0	10-A	
P33/SI00/SB1		
P34/SCK00	8-A	
P35/TCLR1		
P36/TI1/TO11		
P37/TO10	5-A	
P40/AD0-P47/AD7		
P50/AD8-P57/AD15		
P70/ANI0-P77/ANI7	9	Connected to the V _{SS} pin.
P80/TCLR0	8-A	Input state : Each pin is connected to the V _{DD} or V _{SS} pin via a separate resistor. Output state : Open
P81/TI0/TO03		
P82/TO00	5-A	
P83/TO01		
P84/TO02		
P85/TCLRUD	8-A	
P86/PWM0	5-A	
P87/PWM1		
P90/RD		
P91/LWR		
P92/HWR		
P93		

Table 1-1 Input/Output Circuit of Type for Each Pin and Recommended Connection Methods for Unused Pins (2/2)

Pin	I/O circuit type	Recommended connection method
P100/SO10	5-A	Input state : Each pin is connected to the V _{DD} or V _{SS} pin via a separate resistor. Output state : Open
P101/SI10	8-A	
P102/SCK10		
P103/SO11	5-A	
P104/SI11	8-A	
P105/SCK11		
P106/TIUD		
P107/TCUD		
ANO0, ANO1	12	Open
CLKOUT	3	
ASTB	4	
WDTO	19	Connected to the V _{SS} pin.
WAIT	1	Connected to the V _{DD} pin.
MODE0, MODE1	1	-
RESET	2	
AV _{REF1} -AV _{REF3} , AV _{SS}	-	Connected to the V _{SS} pin.
AV _{DD}		Connected to the V _{DD} pin.
NC		Connected to the V _{SS} pin (or open).

Fig. 1-1 Input/Output Circuits of Each Pin



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2. DIFFERENCES BETWEEN THE μPD78P356(A) AND μPD78356(A)

The μPD78P356(A) is produced by replacing the internal mask ROM of the μPD78356(A) with a 48K-byte PROM. Both have the same functions except some differences in ROM specifications, such as write and verify modes. Table 2-1 shows the differences.

In this manual, the functions specific to the μPD78P356(A) are explained. For details of the other functions, refer to the μPD78356(A) document.

Table 2-1 Differences between the μPD78P356(A) and μPD78356(A)

Item	Part number	μPD78P356(A)	μPD78356(A)
Internal program memory (Electrical write)		One-time PROM (Data can be written once)	Mask ROM
ECC circuit		Provided	Not provided
PROM programming terminal		Provided	Not provided
Setting of MODE0 and MODE1		<ul style="list-style-type: none"> • Normal operation mode MODE0, 1 = LL • Programming mode MODE0, 1 = HL • ROM-less mode (with an external 16-bit bus) MODE0, 1 = HH 	<ul style="list-style-type: none"> • Normal operation mode MODE0, 1 = LL • ROM-less mode (with an external 8-bit bus) MODE0, 1 = HL (with an external 16-bit bus) MODE0, 1 = HH
Electrical characteristics		They differ in supply current and other factors.	
Others		Since they differ in circuit scale and mask layout, they differ in noise immunity and noise radiation.	

Cautions 1. The PROM and mask ROM products differ in noise immunity and noise radiation. Use not ES products but CS products (mask ROM products) to evaluate them thoroughly when considering the change from the PROM products to the mask ROM products during processes from preproduction to volume production.

2. Connect the MODE0 and MODE1 pins directly to the V_{DD} or V_{SS} pin.

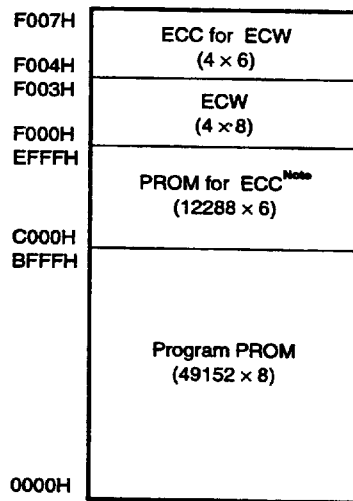
3. PROM PROGRAMMING

The μPD78P356(A) is provided with an electrically writable PROM of 48K × 8 bits for programming and a PROM of 12K × 6 bits for error correcting codes (ECCs).

The ECCs correct errors of the codes written in the programming PROM, improving the reliability of data stored in the PROM.

Fig. 3-1 shows the memory map in the programming mode.

Fig. 3-1 Memory Map in the Programming Mode



Note The six low-order bits are effective in the ECC PROM.

Before programming the PROM, input appropriate signals to the MODE0/V_{PP}, MODE1, P21, and $\overline{\text{RESET}}$ pins to change the mode to the PROM programming mode.

Program the PROM in the same way as for the μPD27C1001A.

To use the ECCs, reset the lowest-order bit (F000.0) in the lowest-order byte of ECW (ECC control word) to enable the ECC circuit operation. The ECW is a 4-byte register for controlling the ECC circuit operation.

The ECCs and ECW are automatically generated by ECCGEN (ECC generator) supplied with the RA78K3 assembler package. (The ECCs are generated in the six low-order bits of the PROM. The two high-order bits are fixed to 1.)

Table 3-1 Pin Functions in Programming Mode

Function	Normal operation mode	Programming mode
Address input	P00-P07, P50, P20, P51-P57	A0-A16
Data input	P40-P47	D0-D7
Program pulse	P12	$\overline{\text{PGM}}$
Chip enable	P10	$\overline{\text{CE}}$
Output enable	P11	$\overline{\text{OE}}$
Program voltage	MODE0/V _{PP}	
Mode control	MODE1, P21, $\overline{\text{RESET}}$	

3.1 OPERATION MODE

To enter the program write/verify mode, set each pin as follows: MODE0/V_{PP} = H, MODE1 = L, P21 = L, $\overline{\text{RESET}}$ = L. In addition, any of the operation modes listed in Table 3-2 can be selected by setting the $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{PGM}}$ pins in this mode.

Set the μPD78P356(A) to the read mode in order to read the contents of PROM.

Handle unused pins according to the caution in PIN CONFIGURATION (2).

Table 3-2 Operation Modes for PROM Programming

Mode	MODE1	P21	$\overline{\text{RESET}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	MODE0/V _{PP}	V _{DD}	D0-D7
Page data latch	L	L	L	H	L	H	+12.5 V	+6.5 V	Data input
Page program				H	H	L			High impedance
Byte program				L	H	L			Data input
Program verify				L	L	H			Data output
Program inhibit				x	L	L			High impedance
				x	H	H			
Read	L	L	L	L	L	H	+5 V	+5 V	Data output
Output disable				L	H	x			High impedance
Standby				H	x	x			High impedance

Remark L : Directly connected to the V_{SS} pin

H : Directly connected to the V_{DD} pin

x : L or H

3.2 PROCEDURE FOR WRITING ON PROM (PAGE PROGRAM MODE)

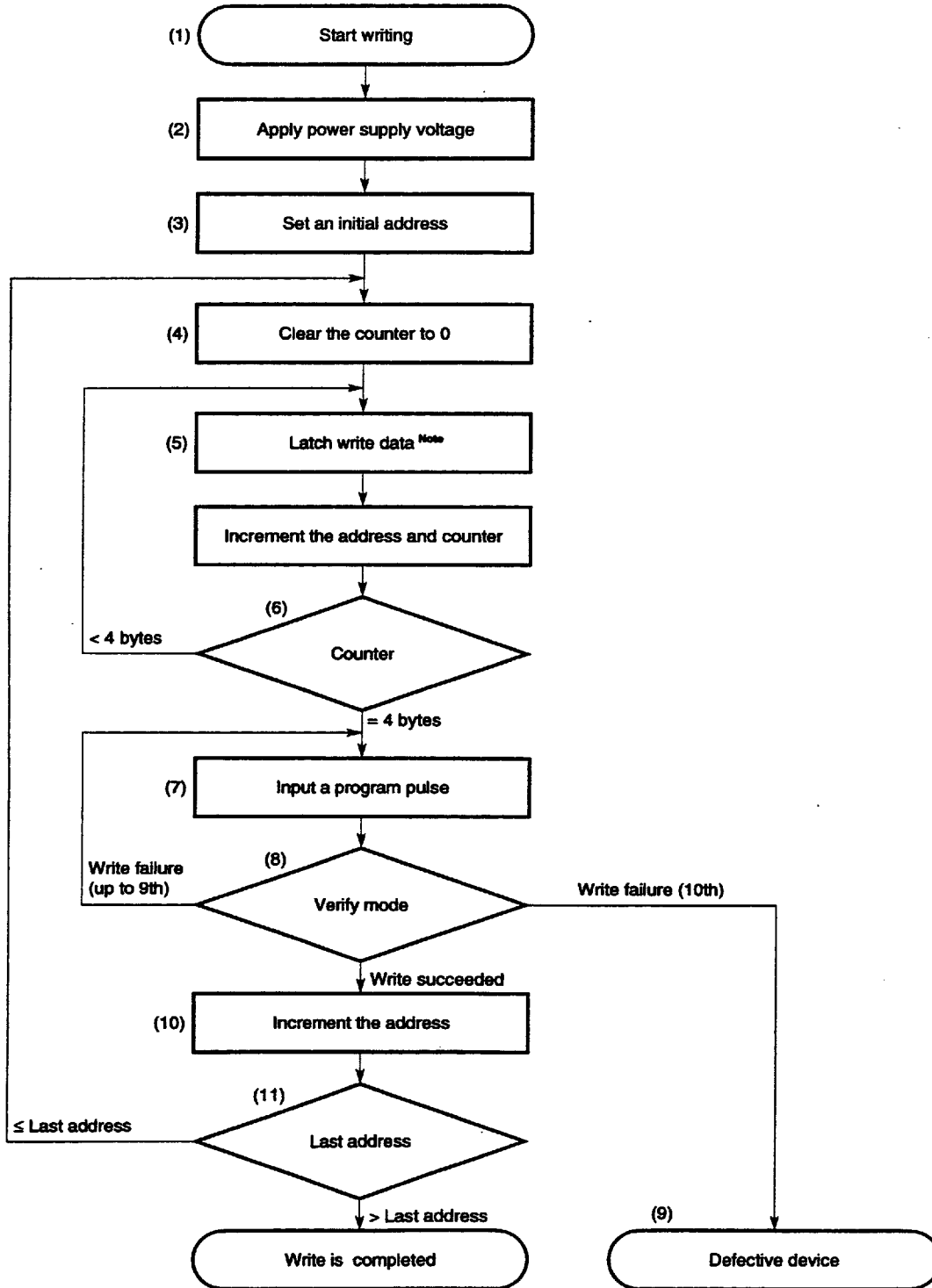
The following is a procedure for writing on PROM. (See Fig. 3-2.)

In the page program mode, data is written in units of pages (four bytes). When write data completes midway of a page, latch FFH after the data so that the data fits into pages.

- (1) Always set each pin as follows: MODE0/V_{PP} = H, MODE1 = L, P21 = L, and $\overline{\text{RESET}}$ = L. Connect unused pins according to PIN CONFIGURATION (2).
- (2) Apply +6.5 V to the V_{DD} pin and +12.5 V to the MODE0/V_{PP} pin.
- (3) Input an initial address to the A0 to A16 pins.
- (4) Clear the page counter.
- (5) Data latch mode. Input write data to the D0 to D7 pins and input an active-low pulse to the $\overline{\text{OE}}$ pin. Increment the address and the page counter.
- (6) Repeat step (5) for a page (four bytes).
- (7) Input a 0.1 ms program pulse (active low) to the $\overline{\text{PGM}}$ pin.
- (8) Verify mode. Checks if data has been written in PROM.
Apply a low level to the $\overline{\text{CE}}$ pin, input an active-low pulse to the $\overline{\text{OE}}$ pin, and then read the write data from the D0 to D7 pins. Repeat this for a page (four bytes). When verification completes, apply a high level to the $\overline{\text{CE}}$ pin.
 - If data has been written, go to step (10).
 - If not, repeat steps (7) and (8). If no data is written yet after the steps have been repeated 10 times, go to step (9).
- (9) Assume the device to be defective and stop write operation.
- (10) Increment the address.
- (11) Repeat steps (4) to (10) until the address exceeds the last address.

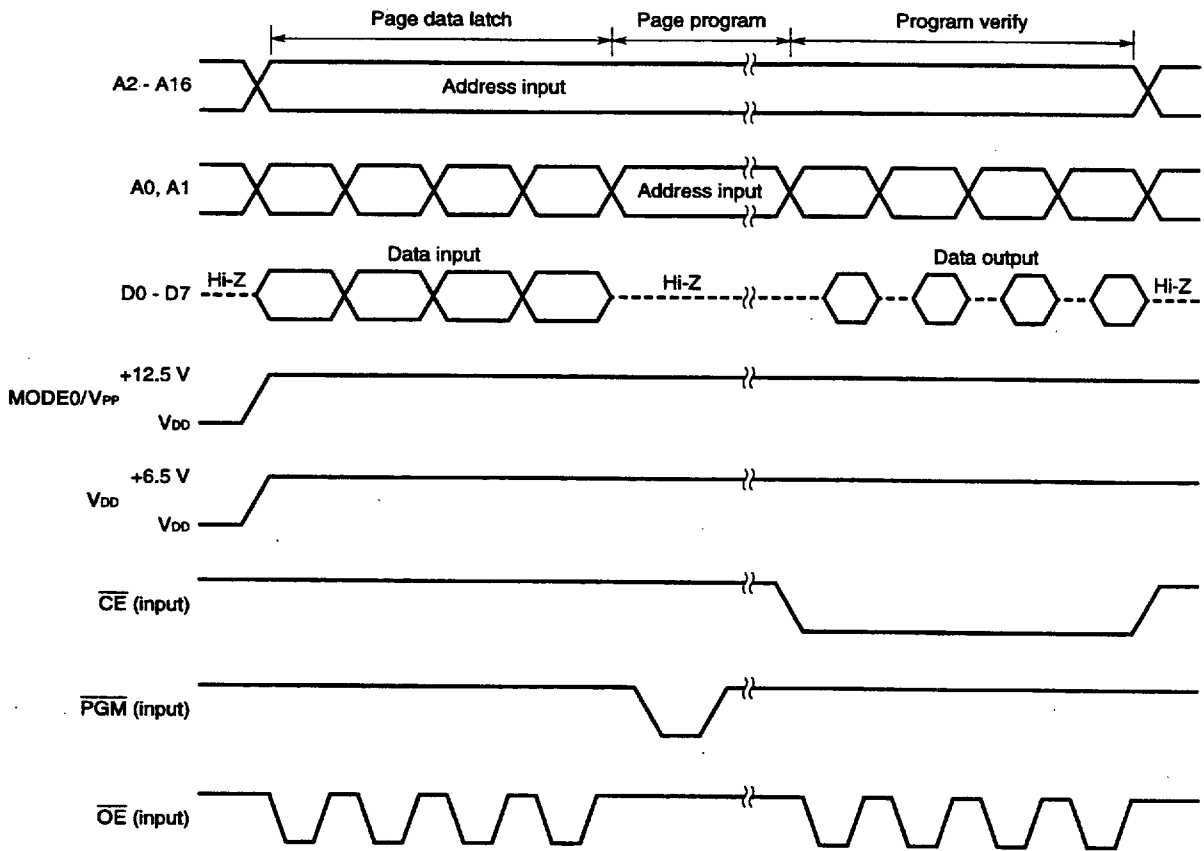
Fig. 3-3 is a timing chart of these steps (2) to (9).

Fig. 3-2 Flowchart of Procedure for Writing (Page Program Mode)



Note If write data does not fill a page, latch FFH for the rest of the page.

Fig. 3-3 PROM Write/Verify Timing Chart (Page Program Mode)



3.3 PROCEDURE FOR WRITING ON PROM (BYTE PROGRAM MODE)

The following is a procedure for writing on PROM. (See Fig. 3-4.)

- (1) Always set each pin as follows: MODE0/V_{PP} = H, MODE1 = L, P21 = L, and $\overline{\text{RESET}}$ = L. Connect unused pins according to PIN CONFIGURATION (2).
- (2) Apply +6.5 V to the V_{DD} pin and +12.5 V to the MODE0/V_{PP} pin, and input a low-level signal to the $\overline{\text{CE}}$ pin.
- (3) Input an initial address to the A0 to A16 pins.
- (4) Input write data to the D0 to D7 pins.
- (5) Input a 0.1 ms program pulse (active low) to the $\overline{\text{PGM}}$ pin.
- (6) Verify mode. Checks if data has been written in PROM.
 - Input an active-low pulse to the $\overline{\text{OE}}$ pin and read the write data from the D0 to D7 pins.
 - If data has been written, go to step (8).
 - If not, repeat steps (4) to (6). If no data is written yet after the steps have been repeated 10 times, go to step (7).
- (7) Assume the device to be defective and stop write operation.
- (8) Increment the address.
- (9) Repeat steps (4) to (8) until the address exceeds the last address.

Fig. 3-5 is a timing chart of these steps (2) to (7).

Fig. 3-4 Flowchart of Procedure for Writing (Byte Program Mode)

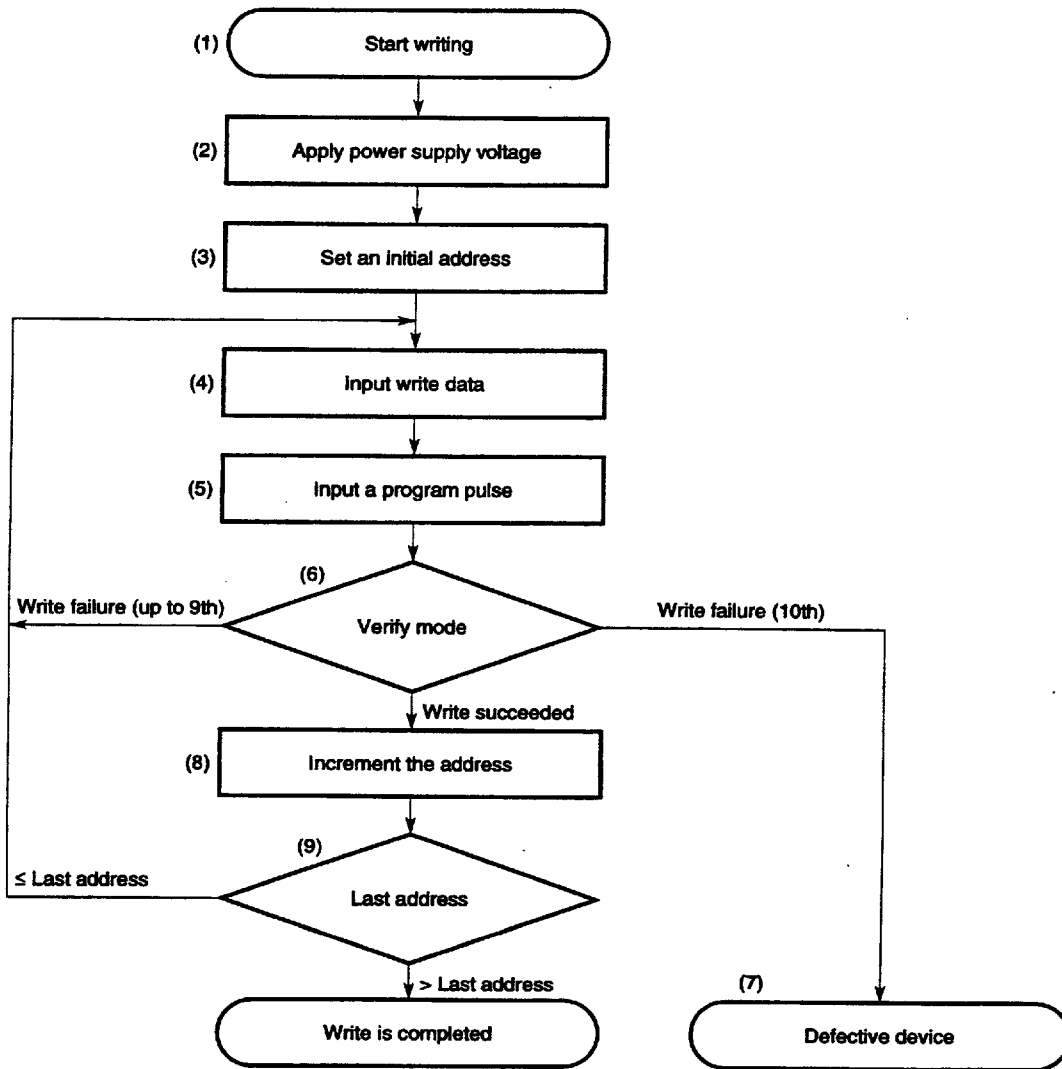
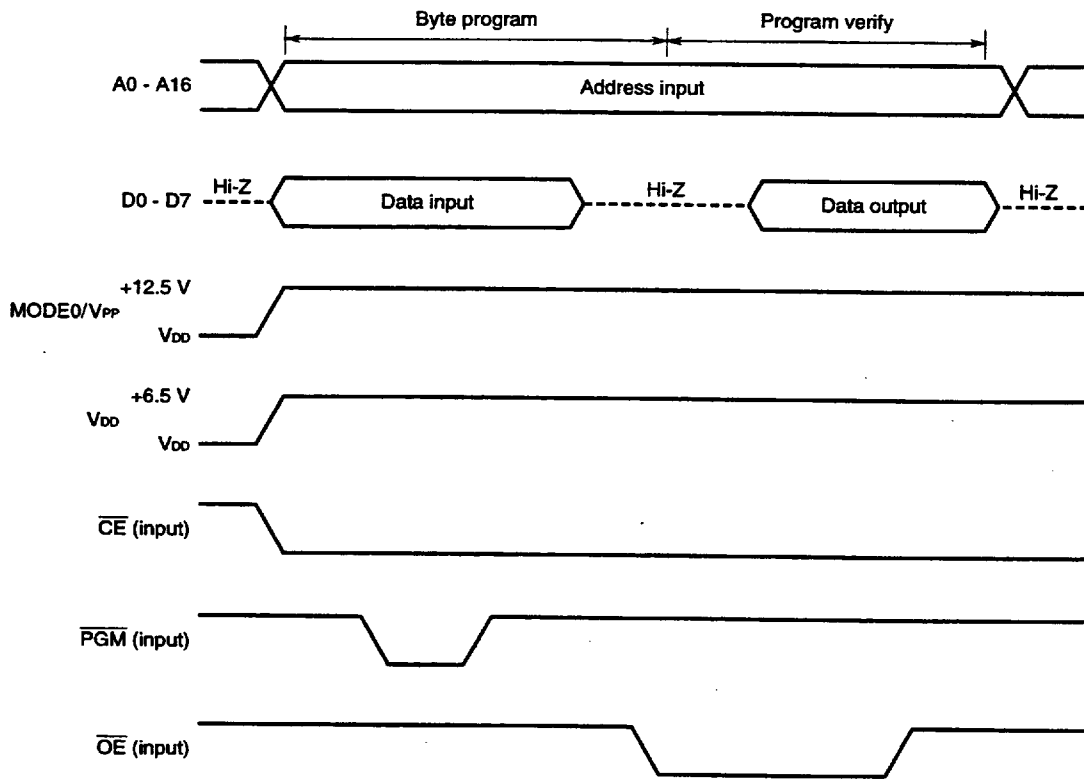


Fig. 3-5 PROM Write/Verify Timing Chart (Byte Program Mode)



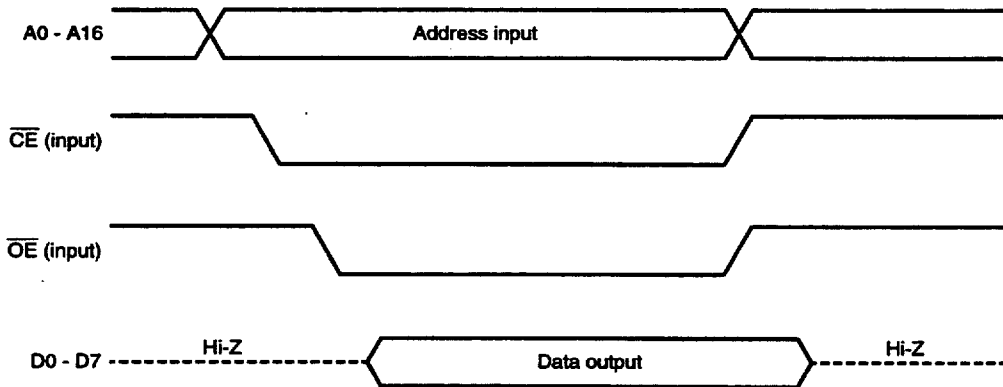
3.4 PROCEDURE FOR READING FROM PROM

The following is a procedure for reading out the contents of PROM to the external data bus (D0 to D7).

- (1) Always set each pin as follows: MODE0/V_{PP} = H, MODE1 = L, P21 = L, and $\overline{\text{RESET}} = \text{L}$. Connect unused pins according to PIN CONFIGURATION (2).
- (2) Apply +5 V to the V_{DD} and MODE0/V_{PP} pins.
- (3) Input the address of data to be read into the A0 to A16 pins.
- (4) Read mode ($\overline{\text{CE}} = \text{L}$, $\overline{\text{OE}} = \text{L}$)
- (5) Output the data on the D0 to D7 pins.

Fig. 3-6 is a timing chart of these steps (2) to (5).

Fig. 3-6 PROM Read Timing Chart



4. SCREENING ONE-TIME PROM PRODUCTS

NEC cannot execute a complete test of one-time PROM products (μ PD78P356GD(A)-5BB) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125 °C for 24 hours.

NEC offers a charged service called QTOP microcomputer service. This service includes writing to one-time PROM, marking, screening, and verification. Ask your sales representative for details.

5. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit	
Supply voltage	V _{DD}		-0.5 to +7.0	V	
	AV _{DD}		-0.5 to V _{DD} + 0.5	V	
	V _{PP}		-0.5 to +13.5	V	
	AV _{SS}		-0.5 to +0.5	V	
Input voltage	V _I	Notes 1, 2	-0.5 to V _{DD} + 0.5	V	
Output voltage	V _O		-0.5 to V _{DD} + 0.5	V	
Low-level output current	I _{OL}	Each pin	4.0	mA	
		Total of all output pins	140	mA	
High-level output current	I _{OH}	Each pin	-1.0	mA	
		Total of all output pins	-30	mA	
Analog input voltage	V _{IAN}	Notes 1, 3	AV _{DD} > V _{DD}	-0.5 to V _{DD} + 0.5	V
			V _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.5	
A/D converter reference input voltage	AV _{REF}		AV _{DD} > V _{DD}	-0.5 to V _{DD} + 0.5	V
			V _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.5	
Operating temperature	T _A		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

- Notes 1. Excluding any overvoltage, which is assumed when determining the characteristics of allowable pin injection current
- 2. For pins other than those described in Note 3
- 3. P70/ANI0 - P77/ANI7

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

CHARACTERISTICS OF ALLOWABLE PIN INJECTION CURRENT WHEN OVERVOLTAGE IS APPLIED
 (T_A = -40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
Positive injection current (V _{IN} > V _{DD})	I _{UH1}	Each pin	Input ports other than ANIn (n = 0 to 7)	Peak value			10	mA
				Average			0.5	mA
	I _{UH2}		ANIn (n = 0 to 7)	Peak value			3	mA
				Average			1	mA
	I _{UH}	Total of all input pins	Peak value				100	mA
			Average				5	mA
Negative injection current (V _{IN} < V _{SS})	I _{UL1}	Each pin	Input ports other than ANIn (n = 0 to 7)	Peak value			-4	mA
				Average				-0.4
	I _{UL2}		ANIn (n = 0 to 7)	Peak value			-4	mA
				Average				-0.3
	I _{UL}	Total of all input pins	Peak value				-40	mA
			Average				-3	mA

- Cautions**
1. If an injection current flows through an analog input pin (ANIn: n = 0 to 7), that current will affect the A/D conversion output corresponding to an input pin adjacent to that pin. In such a case, the A/D conversion output rating for the adjacent pin becomes the normal rating ±2LSB.
 2. The average (absolute value) of the injection current is calculated by the following formula:

$$\text{Average} = \left(\frac{1}{T} \int_0^T |i(t)|^2 dt \right)^{1/2}$$

i(t) is the injection current. The maximum value of |i(t)| is the peak value.

RECOMMENDED OPERATING CONDITIONS

Oscillator frequency	T _A	V _{DD}
8 MHz ≤ f _{osc} ≤ 25 MHz	-40 to +85 °C	+5.0 V ±10 %

CAPACITANCE (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _i	f = 1 MHz 0 V on pins other than measured pins			20	pF
Output capacitance	C _o				20	pF
I/O capacitance	C _{io}				20	pF

OSCILLATOR CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Ceramic resonator or crystal		Oscillator frequency (f _{ox})	8	25	MHz
External clock		X1 input frequency (f _x)	8	25	MHz
		X1 input rising and falling times (t _{rx} , t _{fx})	0	10	ns
		X1 input high-level and low-level widths (t _{wxH} , t _{wxL})	10	115	ns

Caution When using the system clock generator, run wires in the portion surrounded by dotted lines according to the following rules to avoid effects such as stray capacitance:

- Minimize the wiring.
- Never cause the wires to cross other signal lines or run near a line carrying a large varying current.
- Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{ss}. Never connect the capacitor to a ground pattern carrying a large current.
- Never extract a signal from the oscillator.

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Low-level input voltage	V _{IL}		0		0.8	V	
High-level input voltage	V _{IH1}	Note 1	2.2			V	
	V _{IH2}	Note 2	0.8V _{DD}				
Low-level output voltage	V _{OL}	I _{OL} = 2.0 mA			0.45	V	
High-level output voltage	V _{OH}	I _{OH} = -400 μA	V _{DD} - 1.0			V	
Input leakage current	I _{LI}	Note 3	0 V ≤ V _i ≤ V _{DD}			±10	μA
		MODE0/V _{PP}	V _i = V _{DD}			+10	μA
		pin	V _i = 0 V			-200	μA
Analog pin input leakage current	I _{LAN}	Note 4	0 V ≤ V _i ≤ AV _{REF}			±10	μA
Output leakage current	I _{LO}	0 V ≤ V _o ≤ V _{DD}			±10	μA	
V _{DD} supply current	I _{DD1}	Operation mode		70	113	mA	
	I _{DD2}	HALT mode		30	52	mA	
Data retention voltage	V _{DDDR}	STOP mode	2.5			V	
Data retention current	I _{DDDR}	STOP mode	V _{DDDR} = 2.5 V		2	40	μA
			V _{DDDR} = 5.0 V ±10 %		10	100	μA
Software pull-up resistance	R _L	V _i = 0 V	20	40	90	kΩ	

- Notes**
- For pins other than those described in Note 2
 - RESET, X1, X2, P00/RTP0/ADTRG0, P01/RTP1/ADTRG1, P02/RTP2/ADTRG2, P03/RTP3/ADTRG3, P20/NMI, P21/INTP0/TO04, P22/INTP1/TO05, P23/INTP2, P24/INTP3, P25/INTP4, P26/TCLR2/TO21, P27/TO20, P32/SO00/SB0, P33/SI00/SB1, P34/SCK00, P35/TCLR1, P36/TI1/TO11, P80/TCLR0, P81/TI0/TO03, P85/TCLRUD, P101/SI10, P102/SCK10, P104/SI11, P105/SCK11, P106/TIUD, and P107/TCUD
 - For input and input/output pins (excluding MODE0/V_{PP}, X1, X2, and P70/ANI0 to P77/ANI7 being used for analog input.)
 - For P70/ANI0 to P77/ANI7 (only when being used for analog input, during nonsampling operation)

AC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V, C_L = 100 pF, f_{clk} = 25 MHz)

Read/Write Operation (When the General Memory Is Connected)

Parameter	Symbol	Conditions	Min.	Max.	Unit
System clock cycle time	t _{cyk}		80	250	ns
Address setup time (to ASTB ↓)	t _{SAST}		16		ns
Address hold time (to ASTB ↓)	t _{HSTA}		20		ns
Delay from RD ↓ to address float	t _{FRA}			0	ns
Delay from address to data input	t _{DAID}			144	ns
Delay from RD ↓ to data input	t _{DRID}			72	ns
Delay from ASTB ↓ to RD ↓	t _{DSTR}		24		ns
Data hold time (to RD ↑)	t _{HRID}		0		ns
Delay from RD ↑ to address active	t _{DRA}		26		ns
RD low-level width	t _{WRL}		90		ns
ASTB high-level width	t _{WSTH}		23		ns
Delay from LWR, HWR ↓ to data output	t _{DWOD}			30	ns
Delay from ASTB ↓ to LWR, HWR ↓	t _{DSTW}		24		ns
Delay from LWR, HWR ↑ to ASTB ↑	t _{DWST}		105		ns
Data setup time (to LWR, HWR ↑)	t _{SODW}		75		ns
Data hold time (to LWR, HWR ↑)	t _{HWOD}		8		ns
LWR, HWR low-level width	t _{WWL}		90		ns
WAIT setup time (to address)	t _{SAWT}			65	ns
WAIT hold time (to address)	t _{HAWT}		120		ns
WAIT setup time (to ASTB ↓)	t _{SASRY}			24	ns
WAIT hold time (to ASTB ↓)	t _{HASRY}		80		ns
WAIT setup time (to RD ↓)	t _{SRRY}			-25	ns
WAIT setup time (to LWR, HWR ↓)	t _{SWRY}			-25	ns
WAIT hold time (to RD ↓)	t _{HRRY}		31		ns
WAIT hold time (to LWR, HWR ↓)	t _{HWRY}		31		ns
Delay from address to RD ↓	t _{DAR}			95	ns
Delay from address to LWR, HWR ↓	t _{DAW}			95	ns
Delay from WAIT ↑ to data input	t _{DWID}			70	ns
Delay from WAIT ↑ to RD ↑	t _{DWTR}		80		ns
Delay from WAIT ↑ to LWR, HWR ↑	t _{DWTW}		80		ns

tc_{CLK}-Dependent Bus Timing Definition

Symbol	Formula	Min./Max.	Unit
t _{SAST}	$(0.5 + a)T - 24$	Min.	ns
t _{HSTA}	$0.5T - 20$	Min.	ns
t _{WSTH}	$(0.5 + a)T - 17$	Min.	ns
t _{DSTR}	$0.5T - 16$	Min.	ns
t _{WRL}	$(1.5 + n)T - 30$	Min.	ns
t _{DARD}	$(2.5 + a + n)T - 56$	Max.	ns
t _{DRID}	$(1.5 + n)T - 48$	Max.	ns
t _{DRA}	$0.5T - 14$	Min.	ns
t _{DSTW}	$0.5T - 16$	Min.	ns
t _{DWST}	$1.5T - 15$	Min.	ns
t _{WWL}	$(1.5 + n)T - 30$	Min.	ns
t _{DWOD}	$0.5T - 10$	Max.	ns
t _{SODW}	$(1 + n)T - 5$	Min.	ns
t _{SAWT}	$(a + n)T - 15$	Max.	ns
t _{HAWT}	$(0.5 + a + n)T$	Min.	ns
t _{SASRY}	$(n - 0.5)T - 16$	Max.	ns
t _{HASRY}	nT	Min.	ns
t _{SRRY}	$(n - 1)T - 25$	Max.	ns
t _{SWRY}	$(n - 1)T - 25$	Max.	ns
t _{HRRY}	$(n - 0.5)T - 9$	Min.	ns
t _{HWRY}	$(n - 0.5)T - 9$	Min.	ns
t _{DAR}	$(a + 1)T + 15$	Max.	ns
t _{DAW}	$(a + 1)T + 15$	Max.	ns
t _{DWTID}	$T - 10$	Max.	ns
t _{DWTR}	T	Min.	ns
t _{DWTW}	T	Min.	ns

- Remarks**
1. $T = t_{CLK} = 1/f_{CLK}$ (f_{CLK} is the internal system clock frequency.)
 2. When an address wait is inserted, the value of a is 1. Otherwise, it is 0.
 3. The number n represents the number of wait cycles specified by the external wait pin (\overline{WAIT}) or PWC register.
 4. Only the bus timing items listed above are dependent on t_{CLK} .

Serial Operation (T_A = -40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time	t _{CVSK}	$\overline{\text{SCK}}$ output	Internal, divided by 8	640		ns
		$\overline{\text{SCK}}$ input	External clock	640		ns
Serial clock low-level width	t _{WSKL}	$\overline{\text{SCK}}$ output	Internal, divided by 8	280		ns
		$\overline{\text{SCK}}$ input	External clock	280		ns
Serial clock high-level width	t _{WSKH}	$\overline{\text{SCK}}$ output	Internal, divided by 8	280		ns
		$\overline{\text{SCK}}$ input	External clock	280		ns
SI setup time (to $\overline{\text{SCK}}$ ↑)	t _{SRXSK}			80		ns
SI hold time (to $\overline{\text{SCK}}$ ↑)	t _{HSKRX}			80		ns
Delay from $\overline{\text{SCK}}$ ↓ to SO	t _{DSKTX}	R = 1 kΩ, C = 100 pF			110	ns

t_{CVSK}-Dependent Serial Operations

Symbol	Conditions		Formula	Min./Max.	Unit
t _{CVSK}	$\overline{\text{SCK}}$ output	Internal, divided by 8	8T	Min.	ns
	$\overline{\text{SCK}}$ input	External clock	8T	Min.	ns
t _{WSKL}	$\overline{\text{SCK}}$ output	Internal, divided by 8	4T - 40	Min.	ns
	$\overline{\text{SCK}}$ input	External clock	4T - 40	Min.	ns
t _{WSKH}	$\overline{\text{SCK}}$ output	Internal, divided by 8	4T - 40	Min.	ns
	$\overline{\text{SCK}}$ input	External clock	4T - 40	Min.	ns

- Remarks 1. T = t_{CVSK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency.)
 2. The items listed above are dependent on t_{CVSK}.

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Up/Down Counter Operations (T_A = -40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Max.	Unit	
TIUD high/low level width	t _{wTIUH} , t _{wTIUL}	Other than mode 4	NIUD = 0	320		ns
			NIUD = 1	1.28		μs
		Mode 4	NIUD = 0	640		ns
			NIUD = 1	1.28		μs
TCUD high/low level width	t _{wTCUH} , t _{wTCUL}	Other than mode 4	NCUD = 0	320		ns
			NCUD = 1	1.28		μs
		Mode 4	NCUD = 0	640		ns
			NCUD = 1	1.28		μs
TCLRU high/low level width	t _{wTCLUH} , t _{wTCLUL}		NRUD = 0	320		ns
			NRUD = 1	1.28		μs
TCUD setup time (to TIUD ↑)	t _{STCU}	Mode 3	0		ns	
TCUD hold time (to TIUD ↑)	t _{HTCU}	Mode 3	160		ns	
TIUD setup time (to TCUD)	t _{S4TU}	Mode 4	320		ns	
TIUD hold time (to TCUD)	t _{H4TU}	Mode 4	320		ns	
Cycle time for TIUD and TCUD	t _{cyC4}	Mode 4	1.28		μs	

Remark NIUD, NCUD, NRUD: Bits 5, 6, and 7 of the noise protection control register (NPC)

t_{cyk}-Dependent Up/Down Counter Operations

Symbol	Conditions	Formula	Min./Max.	Unit
t _{wTIUH} , t _{wTIUL}	Other than mode 4	NIUD = 0	Min.	ns
		NIUD = 1		
	Mode 4	NIUD = 0		
		NIUD = 1		
t _{wTCUH} , t _{wTCUL}	Other than mode 4	NCUD = 0	Min.	ns
		NCUD = 1		
	Mode 4	NCUD = 0		
		NCUD = 1		
t _{wTCLUH} , t _{wTCLUL}		NRUD = 0	Min.	ns
		NRUD = 1		
t _{HTCU}	Mode 3	2T	Min.	ns
t _{S4TU}	Mode 4	4T	Min.	ns
t _{H4TU}	Mode 4	4T	Min.	ns

Remarks 1. T = t_{cyk} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency.)

2. The items listed above are dependent on t_{cyk}.

3. NIUD, NCUD, NRUD: Bits 5, 6, and 7 of the noise protection control register (NPC)

Other Operations (T_A = -40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Max.	Unit
NMI high/low level width	t _{WNH} , t _{WNL}	No analog noise	2		μs
INTP0 high/low level width	t _{WI0H} , t _{WI0L}		320		ns
INTP1 high/low level width	t _{WI1H} , t _{WI1L}		320		ns
INTP2 high/low level width	t _{WI2H} , t _{WI2L}		320		ns
INTP3 high/low level width	t _{WI3H} , t _{WI3L}		320		ns
INTP4 high/low level width	t _{WI4H} , t _{WI4L}		320		ns
TIO high/low level width	t _{WI0H} , t _{WI0L}	NIO = 0	320		ns
		NIO = 1	1.28		μs
TI1 high/low level width	t _{WI1H} , t _{WI1L}	NI1 = 0	320		ns
		NI1 = 1	1.28		μs
TCLR0 high/low level width	t _{WTCL0H} , t _{WTCL0L}	NR0 = 0	320		ns
		NR0 = 1	1.28		μs
TCLR1 high/low level width	t _{WTCL1H} , t _{WTCL1L}	NR1 = 0	320		ns
		NR1 = 1	1.28		μs
TCLR2 high/low level width	t _{WTCL2H} , t _{WTCL2L}	NR2 = 0	320		ns
		NR2 = 1	1.28		μs
RESET high/low level width	t _{WRSH} , t _{WRSL}	No analog noise	1.5		μs

Remark NIO, NI1 : Bits 0 and 2 of the noise protection control register (NPC)
 NR0, NR1, NR2: Bits 1, 3, and 4 of the noise protection control register (NPC)

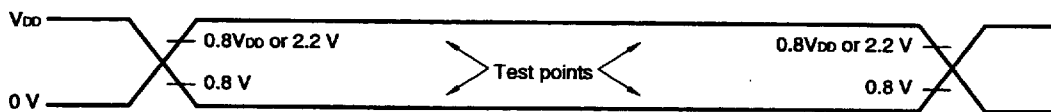
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Other t_{cyk}-Dependent Operations

Symbol	Conditions	Formula	Min./Max.	Unit
t _{W0H} , t _{W0L}		4T	Min.	ns
t _{W1H} , t _{W1L}		4T	Min.	ns
t _{W2H} , t _{W2L}		4T	Min.	ns
t _{W3H} , t _{W3L}		4T	Min.	ns
t _{W4H} , t _{W4L}		4T	Min.	ns
t _{W70H} , t _{W70L}	NI0 = 0	4T	Min.	ns
	NI0 = 1	16T		
t _{W71H} , t _{W71L}	NI1 = 0	4T	Min.	ns
	NI1 = 1	16T		
t _{W7C0H} , t _{W7C0L}	NR0 = 0	4T	Min.	ns
	NR0 = 1	16T		
t _{W7C1H} , t _{W7C1L}	NR1 = 0	4T	Min.	ns
	NR1 = 1	16T		
t _{W7C2H} , t _{W7C2L}	NR2 = 0	4T	Min.	ns
	NR2 = 1	16T		

- Remarks 1. $T = t_{cyk} = 1/f_{CLK}$ (f_{CLK} is the internal system clock frequency.)
 2. The bus timing items listed above are dependent on t_{cyk} .
 3. NI0, NI1 : Bits 0 and 2 of the noise protection control register (NPC)
 NR0, NR1, NR2: Bits 1, 3, and 4 of the noise protection control register (NPC)

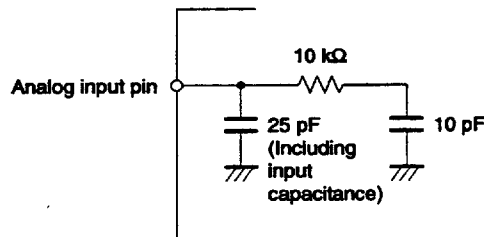
AC Timing Test Points



A/D CONVERTER CHARACTERISTICS (T_A = -40 to +85 °C, AV_{DD} = V_{DD} = +5 V ±10 %, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			10			bit
Total error ^{Note 1}		4.5 V ≤ AV _{REF1} ≤ AV _{DD}			±0.4	%FSR
		3.4 V ≤ AV _{REF1} ≤ AV _{DD}			±0.7	%FSR
Quantization error					±1/2	LSB
Conversion time	t _{CONV}	A/D trigger mode	2			μs
		Timer trigger mode, external trigger mode	2 + 5T			μs
Sampling time	t _{SAMP}	t _{cyk} = 80.0 ns	5.5			t _{cyk}
Zero-scale calibration ^{Note 1}		4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±2.5	LSB
		3.4 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5	LSB
Full scale calibration ^{Note 1}		4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±3.0	LSB
		3.4 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5	LSB
Nonlinearity calibration ^{Note 1}		4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±2.5	LSB
		3.4 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5	LSB
Analog input voltage ^{Note 2}	V _{IAN}		-0.3		AV _{REF1} + 0.3	V
Analog input impedance	R _{AN}	Nonsampling		10		MΩ
		Sampling		Note 3		
Reference voltage	AV _{REF1}		3.4		AV _{DD}	V
AV _{REF1} current	AI _{REF1}			3.0	8.0	mA
AV _{DD} supply current	AI _{DD}	Operation mode		3.3	13.0	mA
A/D converter data retention current	AI _{DDDR}	STOP mode	AV _{DDDR} = 2.5 V	2	10	μA
			AV _{DDDR} = 5 V ±10 %	10	50	μA

- Notes**
- Quantization error is excluded.
 - When -0.3 V ≤ V_{IAN} ≤ 0 V, the conversion result is 000H.
When 0 V < V_{IAN} < AV_{REF1}, the voltage is converted with a 10-bit resolution.
When AV_{REF1} ≤ V_{IAN} ≤ AV_{REF1} + 0.3 V, the conversion result is 3FFH.
 - During sampling, the analog input impedance is equal to that of the following equivalent circuit.
(The figure below shows typical values. These values may not be correct for your application.)



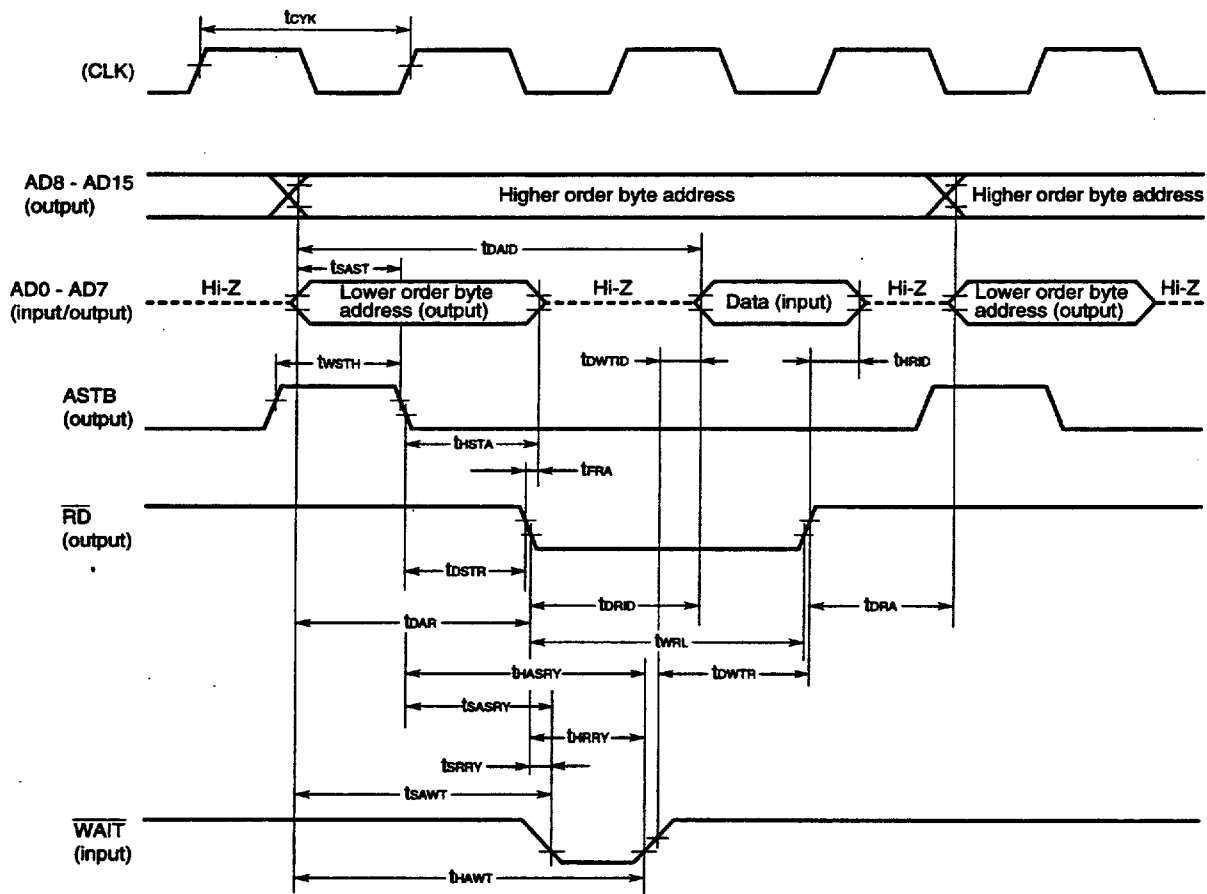
Remark T = t_{cyk} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency.)

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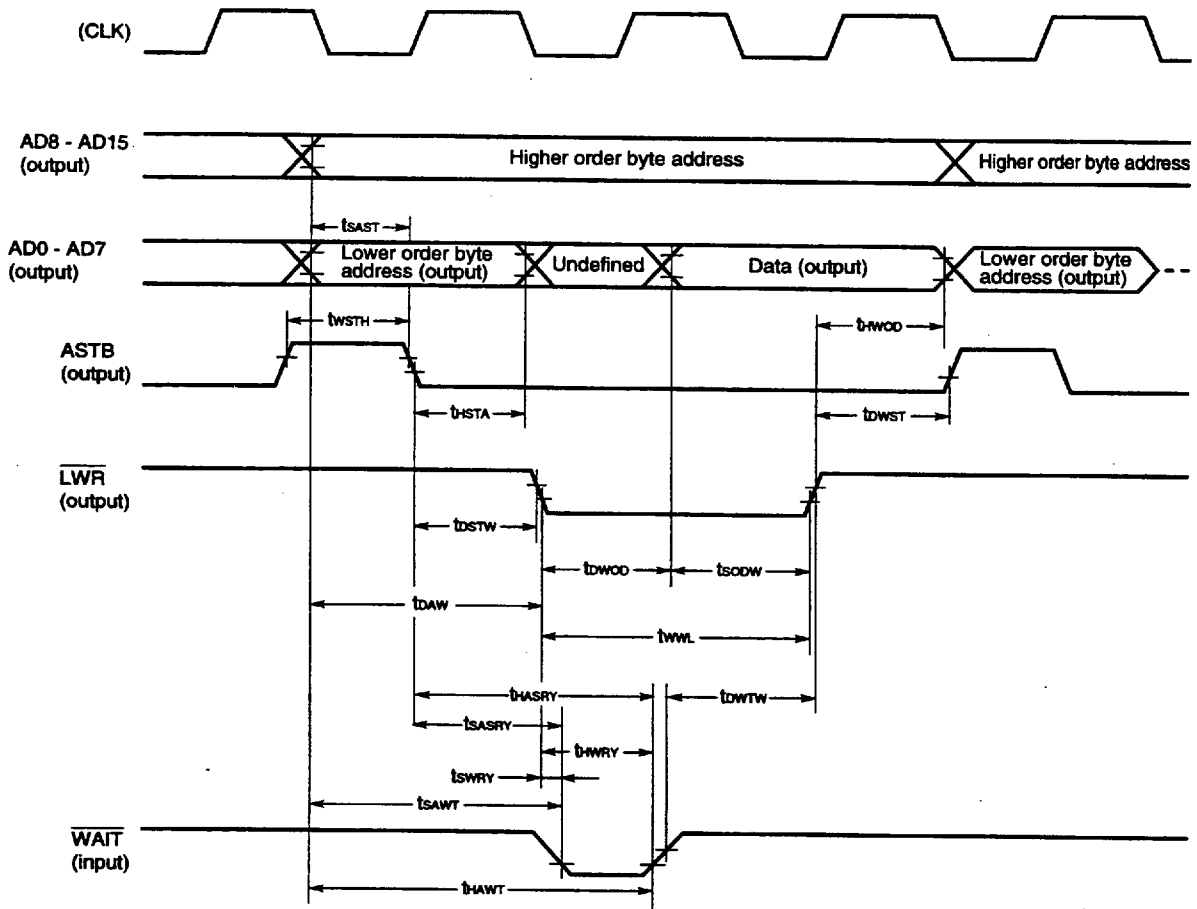
D/A CONVERTER CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $AV_{REF2} = V_{DD} = +5$ V ± 10 %, $AV_{REF3} = V_{SS} = 0$ V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution					8	bit
Total error		$AV_{REF2} = V_{DD} = +5$ V, $AV_{REF3} = V_{SS} = 0$ V			± 0.4	%
Settling time		Load: 2 M Ω , 30 pF			2	μ s
Output resistance	R_o	DACS0, DACS1 = 7FH		10		k Ω
Analog reference voltage	AV_{REF2}		0.75 V_{DD}		V_{DD}	V
Analog reference voltage	AV_{REF3}		V_{SS}		0.2 V_{DD}	V
Reference power supply input current	AI_{REF2}		0		5	mA
Reference power supply input current	AI_{REF3}		-5		0	mA

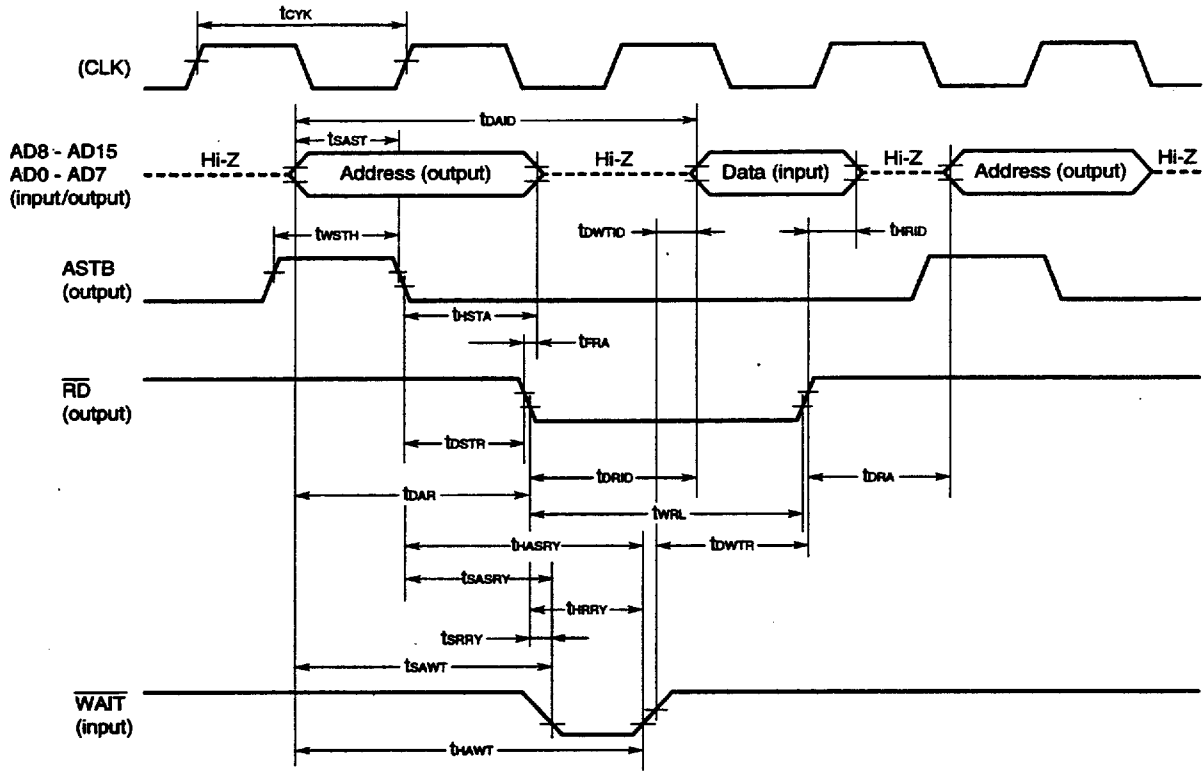
Read Operation (for 8-bit)



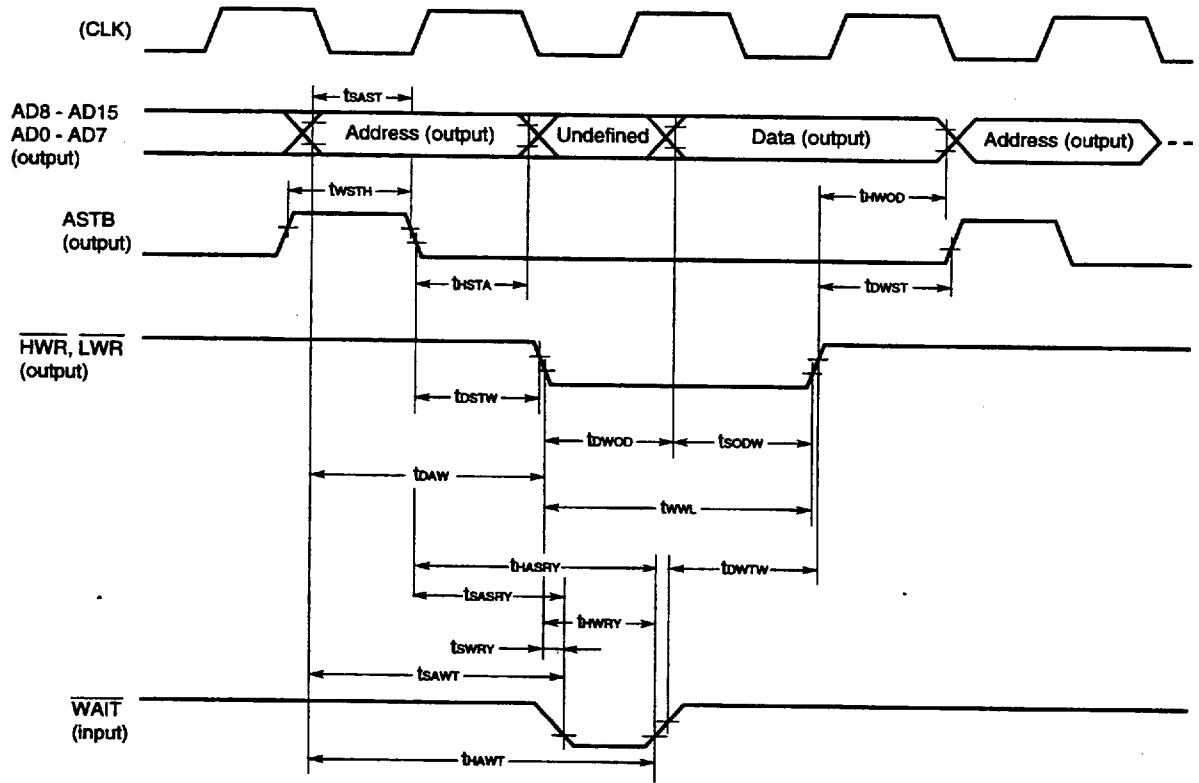
Write Operation (for 8-bit)



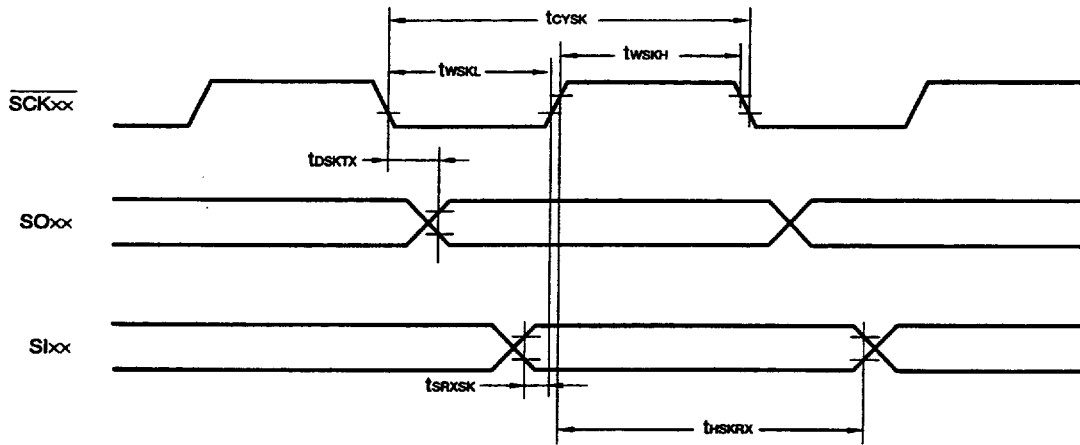
Read Operation (for 16-bit)



Write Operation (for 16-bit)

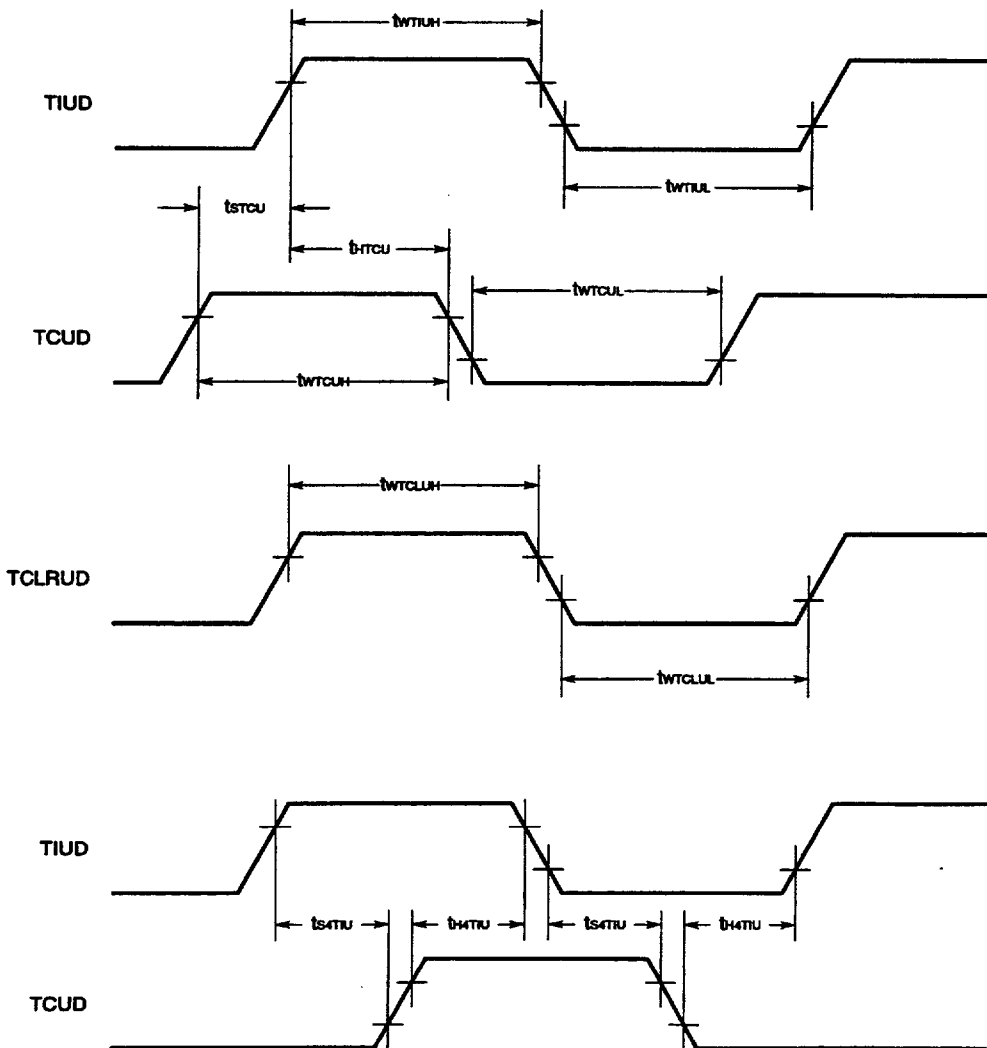


Serial Operation

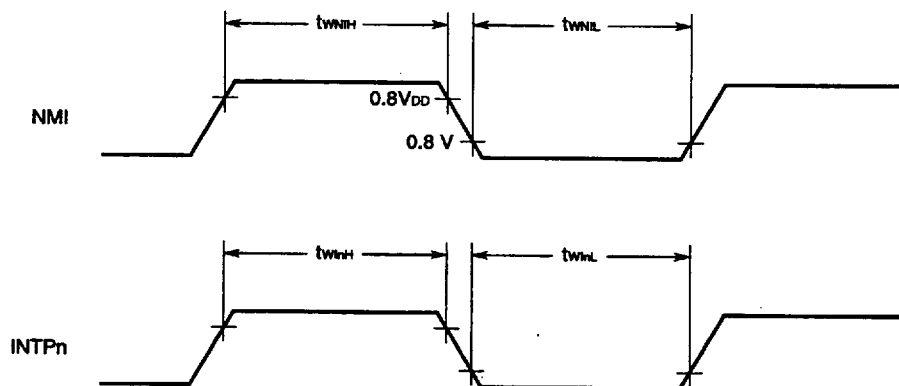


Remark xx: 00, 10, or 11

Up/Down Counter Input Timing

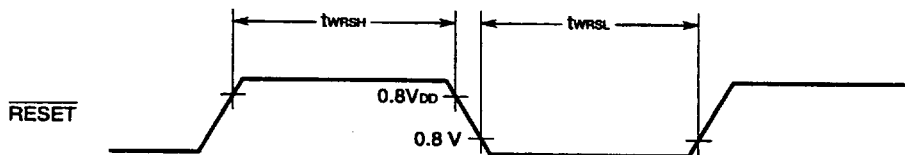


Interrupt Input Timing

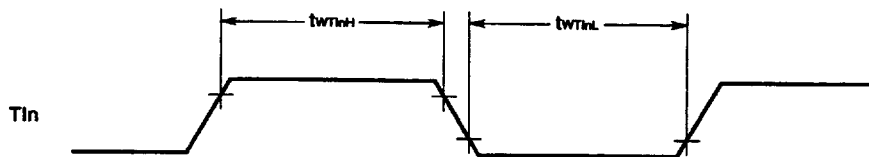


Remark n = 0 to 4

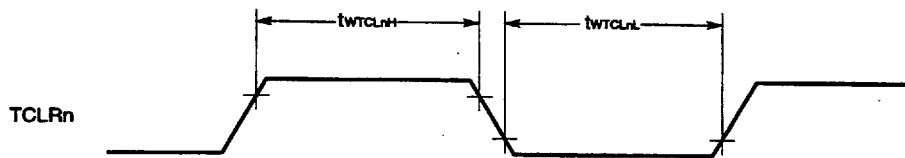
Reset Input Timing



Timer Pin Input Timing



Remark n = 0 or 1



Remark n = 0 to 2

DC PROGRAMMING CHARACTERISTICS (T_A = 25 ±5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol ^{Note 1}	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V _{IH}	V _{IH}		2.2		V _{DDP} + 0.3	V
Low-level input voltage	V _{IL}	V _{IL}		-0.3		0.8	V
Input leakage current	I _{IIP}	I _I	0 ≤ V _I ≤ V _{DDP} ^{Note 2}			±10	μA
High-level output voltage	V _{OH}	V _{OH}	I _{OH} = -400 μA	2.4			V
Low-level output voltage	V _{OL}	V _{OL}	I _{OL} = 2.1 mA			0.45	V
Input current	I _{AS}	-	A9 (P20/NMI) pin			±10	μA
Output leakage current	I _{LO}	-	0 ≤ V _O ≤ V _{DDP} , $\overline{OE} = V_{IH}$			±10	μA
V _{DDP} supply voltage	V _{DDP}	V _{CC}	Program memory write mode	6.25	6.5	6.75	V
			Program memory read mode	4.5	5.0	5.5	V
V _{PP} supply voltage	V _{PP}	V _{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V _{PP} = V _{DDP}			V
V _{DDP} supply current	I _{DD}	I _{DD}	Program memory write mode			30	mA
			Program memory read mode			100	mA
V _{PP} supply current	I _{PP}	I _{PP}	Program memory write mode			50	mA
			Program memory read mode		1.0	100	μA

Notes 1. Symbols for the corresponding μPD27C1001A

2. The V_{DDP} represents the V_{DD} pin as viewed in the programming mode.

AC PROGRAMMING CHARACTERISTICS (T_A = 25 ±5 °C, V_{SS} = 0 V)

PROM Write Mode (Page Program Mode)

Parameter	Symbol ^{Note 1}	Conditions	Min.	Typ.	Max.	Unit
Address set up time	t _{AS}		2			μs
$\overline{\text{CE}}$ set time	t _{CES}		2			μs
Input data setup time	t _{DS}		2			μs
Address hold time	t _{AH}		2			μs
	t _{AHL}		2			μs
	t _{AHV}		0			μs
Input data hold time	t _{DH}		2			μs
Output data hold time	t _{DF}		0		250	ns
V _{PP} setup time	t _{VPS}		2			μs
V _{DDP} setup time	t _{VDS} ^{Note 2}		2			μs
Initial program pulse width	t _{PW}		0.095	0.1	0.105	ms
$\overline{\text{OE}}$ set time	t _{OES}		2			μs
Valid data delay time from $\overline{\text{OE}}$	t _{OE}				1.0	μs
$\overline{\text{OE}}$ pulse width in the data latch	t _{LW}		1			μs
PGM setup time	t _{PGMS}		2			μs
$\overline{\text{CE}}$ hold time	t _{CEH}		2			μs
$\overline{\text{OE}}$ hold time	t _{OEH}		2			μs

Notes 1. These symbols (except t_{VDS}) correspond to those of the μPD27C1001A.

2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

PROM Write Mode (Byte Program Mode)

Parameter	Symbol ^{Note 1}	Conditions	Min.	Typ.	Max.	Unit
Address set up time	t _{AS}		2			μs
\overline{CE} set time	t _{CES}		2			μs
Input data setup time	t _{DS}		2			μs
Address hold time	t _{AH}		2			μs
Input data hold time	t _{DH}		2			μs
Output data hold time	t _{DF}		0		250	ns
V _{PP} setup time	t _{VPS}		2			μs
V _{DDP} setup time	t _{VDS} ^{Note 2}		2			μs
Initial program pulse width	t _{PW}		0.095	0.1	0.105	ms
\overline{OE} set time	t _{OES}		2			μs
Valid data delay time from \overline{OE}	t _{OE}				1.0	μs

Notes 1. These symbols (except t_{VDS}) correspond to those of the μPD27C1001A.

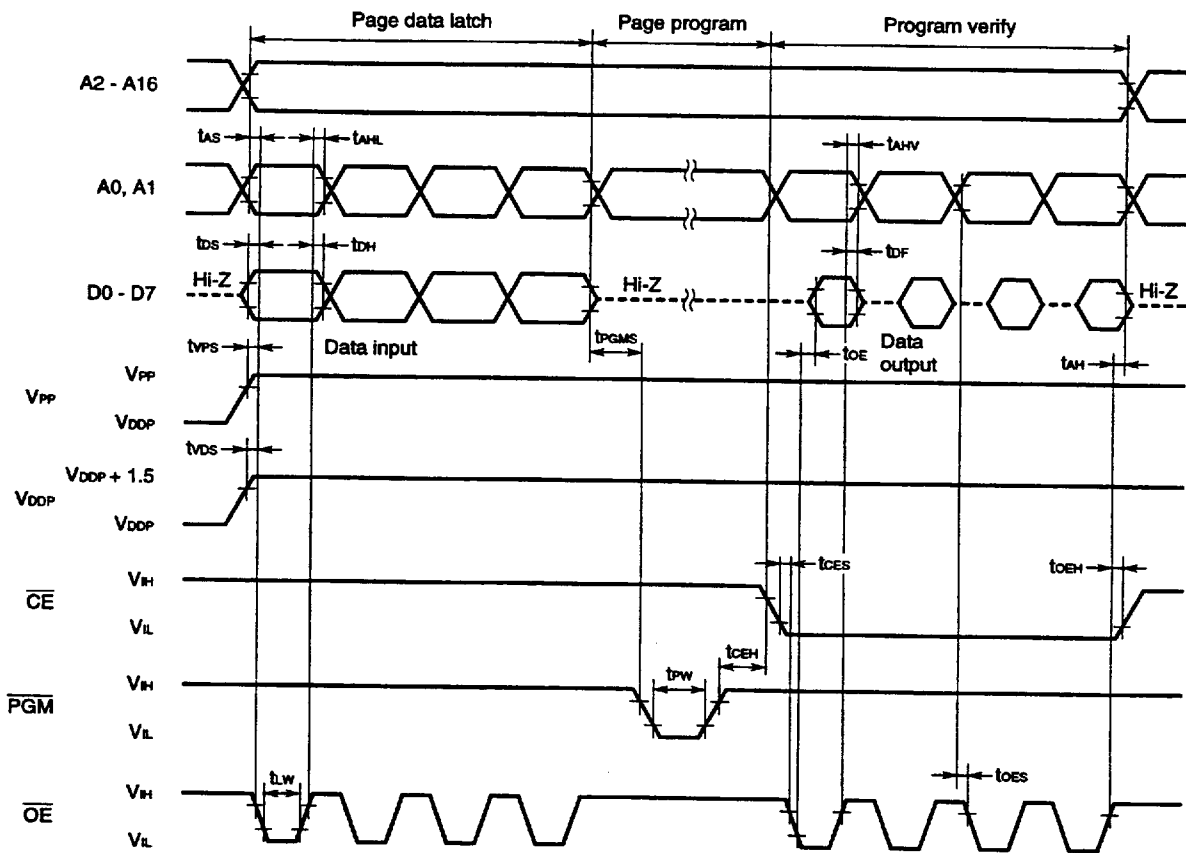
2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

PROM Read Mode

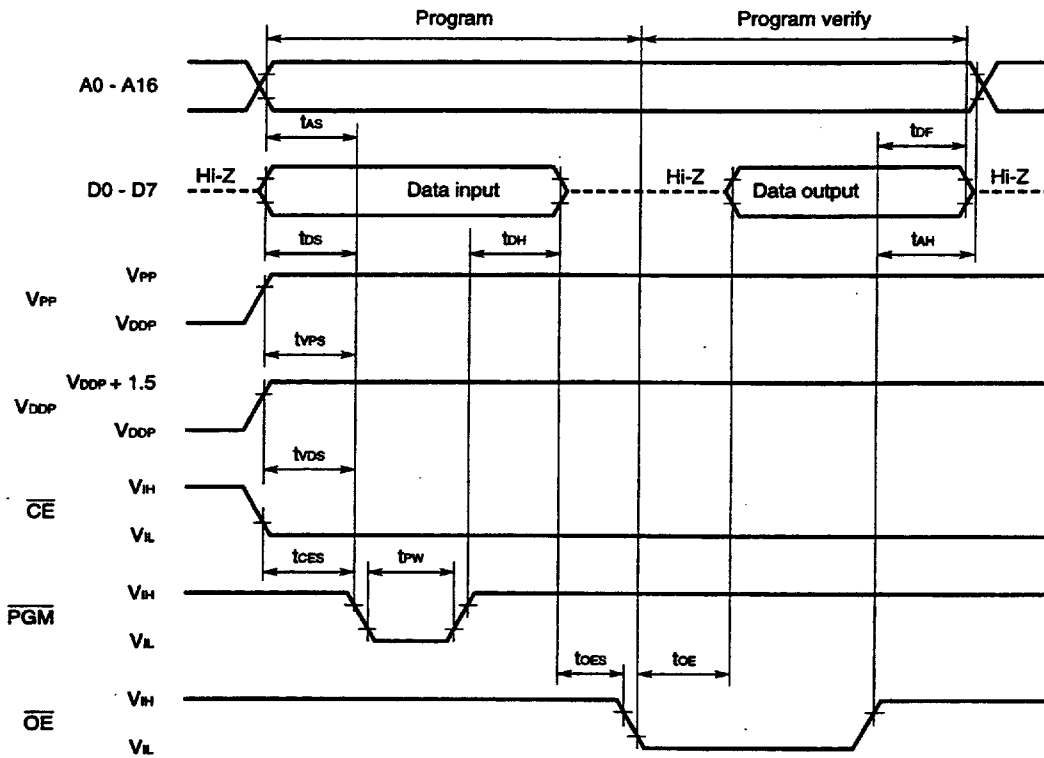
Parameter	Symbol ^{Note}	Conditions	Min.	Typ.	Max.	Unit
Data output time from address	t _{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			1.0	μs
$\overline{CE} \downarrow \rightarrow$ data output time	t _{CE}	$\overline{OE} = V_{IL}$			1.0	μs
$\overline{OE} \downarrow \rightarrow$ data output time	t _{OE}	$\overline{CE} = V_{IL}$			1.0	μs
Data hold time to $\overline{OE} \uparrow$	t _{DF}	$\overline{CE} = V_{IL}$	0		250	ns
Data hold time to address	t _{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note These symbols correspond to those of the μPD27C1001A.

PROM Write Mode Timing (Page Program Mode)

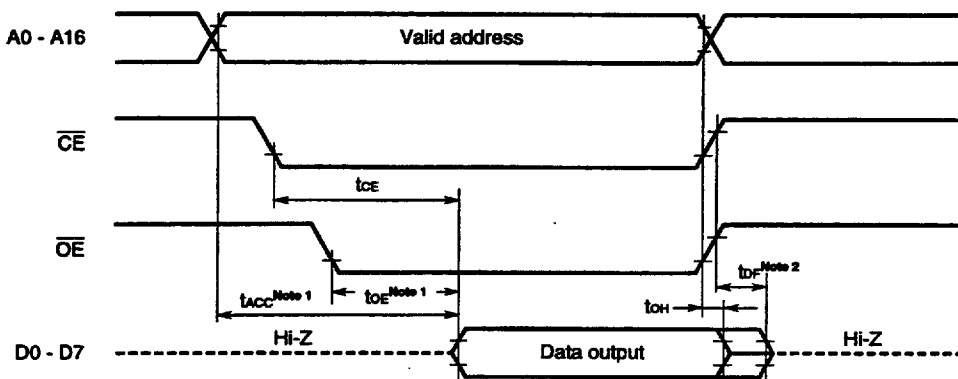


PROM Write Mode Timing (Byte Program Mode)



- Cautions 1.** V_{DDP} must be applied before V_{PP} , and must be cut after V_{PP} .
- 2.** V_{PP} including overshoot must not exceed +13.5 V.
- 3.** Plugging in or out the board with the V_{PP} pin supplied with 12.5 V may adversely affect its reliability.

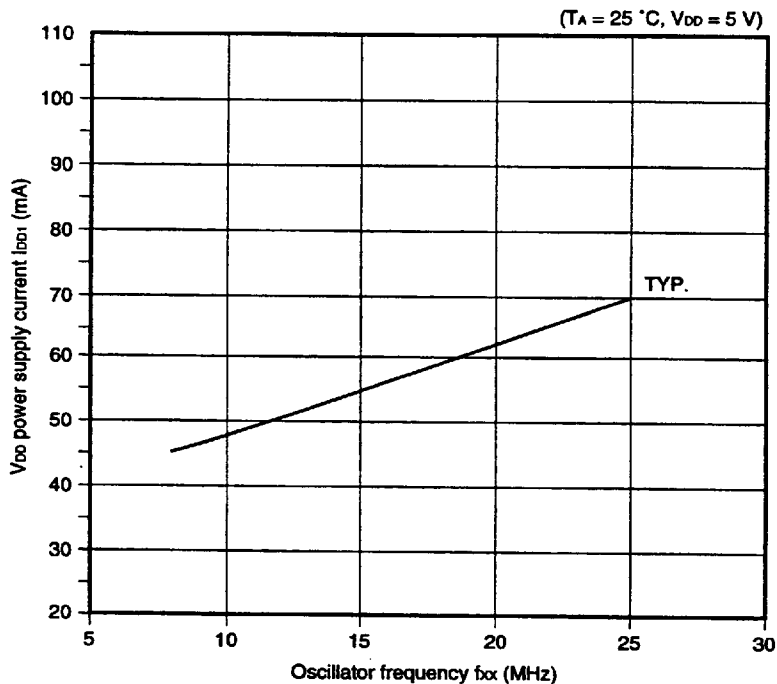
PROM Read Mode Timing



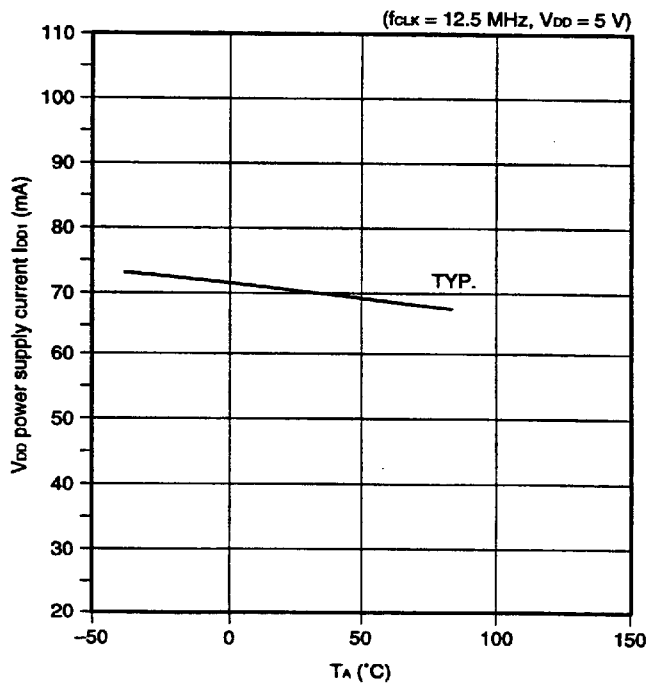
- Notes 1.** For reading within t_{ACC} , the delay of the \overline{OE} input from falling edge of \overline{CE} must be within $t_{ACC} - t_{OE}$.
- 2.** t_{DF} is the time measured from when either \overline{OE} or \overline{CE} reaches V_{IH} , whichever is faster.

6. CHARACTERISTIC CURVES (FOR REFERENCE)

I_{DD1} vs f_{osc}

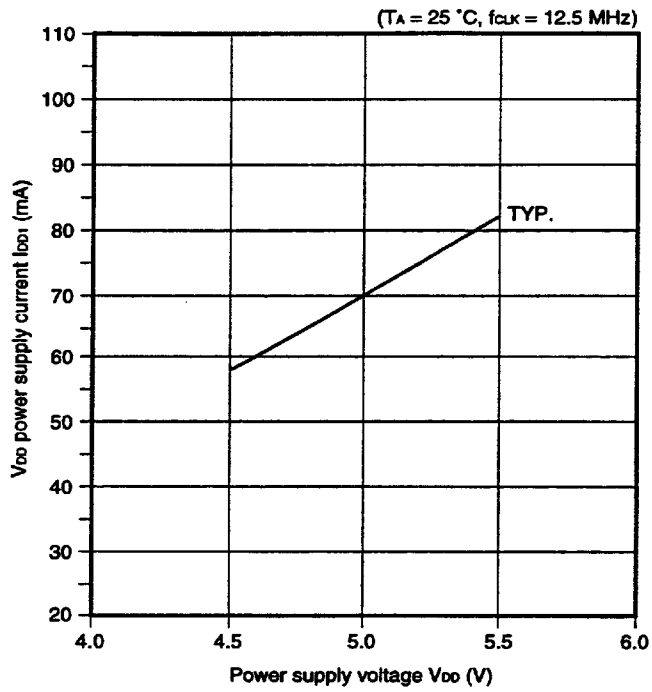


I_{DD1} vs T_A

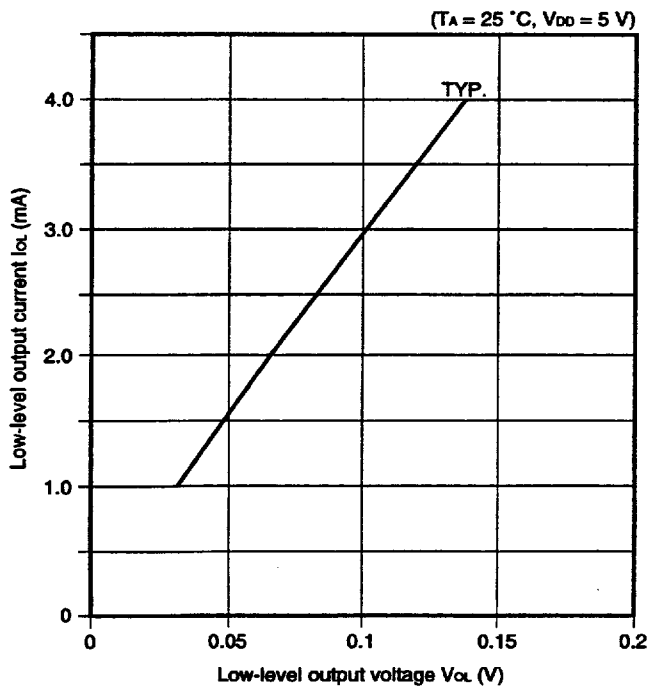


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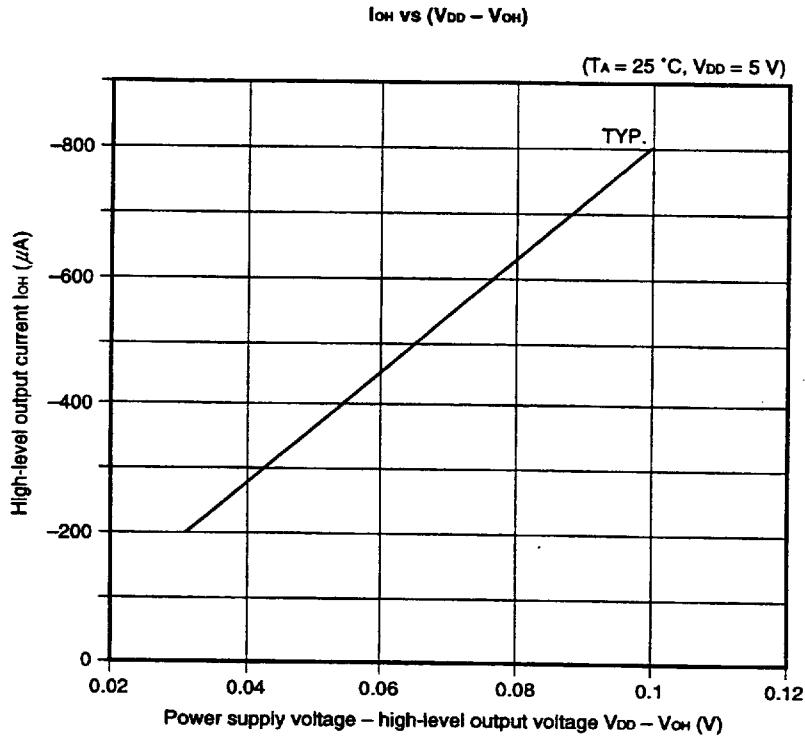
I_{DD1} vs V_{DD}



I_{OL} vs V_{OL}



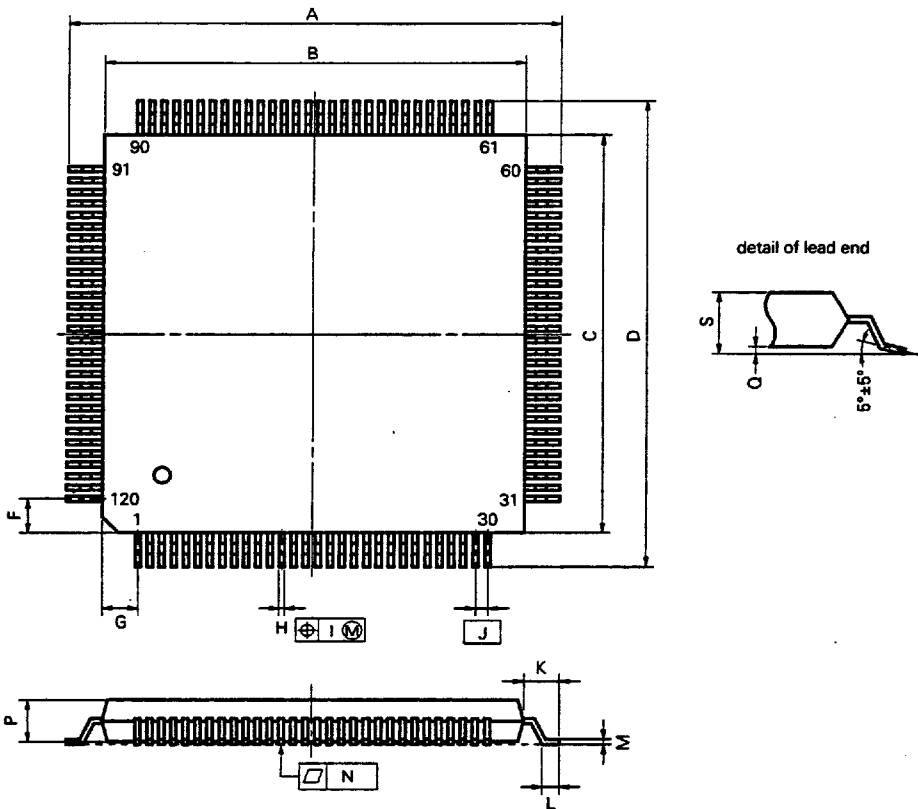
■ 6427525 0084727 711 ■



■ 6427525 0084728 658 ■

7. PACKAGE DRAWINGS

120 PIN PLASTIC QFP (□28)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P120GD-80-5BB-3

ITEM	MILLIMETERS	INCHES
A	32.0±0.4	1.260±0.016
B	28.0±0.2	1.102 ^{+0.009} _{-0.008}
C	28.0±0.2	1.102 ^{+0.009} _{-0.008}
D	32.0±0.4	1.260±0.016
F	2.4	0.094
G	2.4	0.094
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	2.0±0.2	0.079 ^{+0.009} _{-0.008}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
S	4.0 MAX.	0.157 MAX.

8. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD78P356(A).

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 8-1 Soldering Conditions for Surface-Mount Devices

μPD78P356GD(A)-5BB: 120-pin plastic QFP (28 × 28 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (at 210 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit ^{Note} : 7 days (36 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	IR35-367-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit ^{Note} : 7 days (36 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	VP15-367-2
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature : 120 °C max. (measured on the package surface) Exposure limit ^{Note} : 7 days (36 hours of pre-baking is required at 125 °C afterward.)	WS60-367-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	-

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

APPENDIX A TOOLS

A.1 DEVELOPMENT TOOLS

The following tools are provided for developing a system that uses the μPD78P356(A):

Language processor

78K/III series relocatable assembler (RA78K3)	This relocatable program can be used for all 78K/III series emulators. With its macro functions, it allows the user to improve program development efficiency. A structured-programming assembler is also provided, which enables explicit description of program control structures. This assembler could improve productivity in program production and maintenance.			
	Host machine	OS	Distribution media	
	PC-9800 series	MS-DOSTM	3.5-inch 2HD	μS5A13RA78K3
			5.25-inch 2HD	μS5A10RA78K3
	IBM PC/AT™ or compatibles	PC DOS™	3.5-inch 2HC	μS7B13RA78K3
			5.25-inch 2HC	μS7B10RA78K3
	HP9000 series 700™	HP-UXTM	DAT	μS3P16RA78K3
	SPARCstation™	SunOSTM	Cartridge tape (QIC-24)	μS3K15RA78K3
NEWS™	NEWS-OSTM	μS3R15RA78K3		
78K/III series C compiler (CC78K3)	This C compiler can be used for all 78K/III series emulators. The compiler converts programs written in C language into object codes executable on the microcomputer. When the compiler is used, the 78K/III series relocatable assembler package (RA78K3) is needed.			
	Host machine	OS	Distribution media	
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13CC78K3
			5.25-inch 2HD	μS5A10CC78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13CC78K3
			5.25-inch 2HC	μS7B10CC78K3
	HP9000 series 700	HP-UX	DAT	μS3P16CC78K3
	SPARCstation	SunOS	Cartridge tape (QIC-24)	μS3K15CC78K3
NEWS	NEWS-OS	μS3R15CC78K3		

Remark It is guaranteed that the relocatable assembler and C compiler run only under the OSs on the corresponding host machines described above.

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PROM programming tools

Hardware	PG-1500	The PG-1500 PROM programmer is used together with an accessory board and optional program adapter. It allows the user to program a single chip microcomputer containing PROM independently or from a host machine. The PG-1500 can be used to program typical 256K-bit to 4M-bit PROMs.			
	PA-78P356GD	Programmer adapter for writing programs to the μPD78P356(A). Used with a PROM programmer such as the PG-1500. PA-78P356GD : For μPD78P356GD(A)			
Software	PG-1500 controller	This program enables the host machine to control the PG-1500 through the serial and parallel interfaces.			
		Host machine	OS	Distribution media	Part number
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13PG1500
				5.25-inch 2HD	μS5A10PG1500
		IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13PG1500
5.25-inch 2HC	μS7B10PG1500				

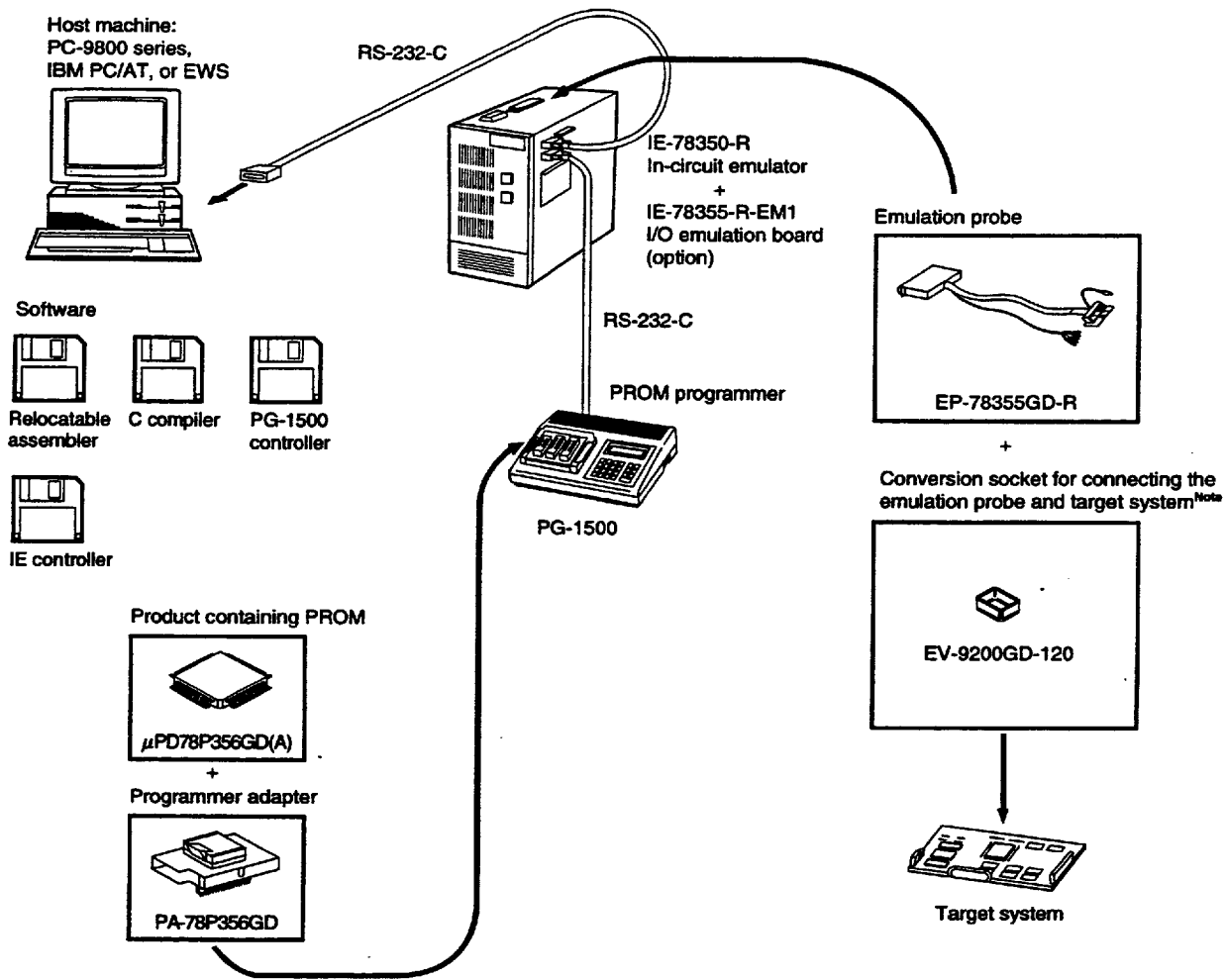
Remark It is guaranteed that the PG-1500 controller runs only under the OSs on the corresponding host machines described above.

Debugging tools (when the IE controller is used)

Hardware	IE-78350-R	In-circuit emulator for developing and debugging an application system. For debugging, connect the emulator to the host machine.			
	IE-78355-R-EM1	I/O emulation board for emulating peripheral hardware such as the I/O ports of the target device.			
	EP-78355GD-R EV-9200GD-120	Emulation probe for connecting the IE-78350-R to the target system. The EV-9200GD-120 conversion socket is supplied with the emulation probe, to connect the target system.			
Software	IE-78350-R control program (IE controller)	This control program allows the user to control the IE-78350-R from the host machine. Its automatic command execution function ensures more efficient debugging.			
		Host machine	OS	Distribution media	Part number
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13IE78355
				5.25-inch 2HD	μS5A10IE78355
		IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13IE78355
5.25-inch 2HC	μS7B10IE78355				

Remark It is guaranteed that the IE controller runs only under the OSs on the corresponding host machines described above.

Development tool configuration (when the IE controller is used)



Note The conversion socket is supplied with the emulation probe.

- Remarks 1.** The PG-1500 can be directly connected to the host machine via the RS-232-C interface.
2. In this figure, a 3.5-inch floppy disk is shown as an example distribution medium for the software.

Debugging tools (when the integrated debugger is used)

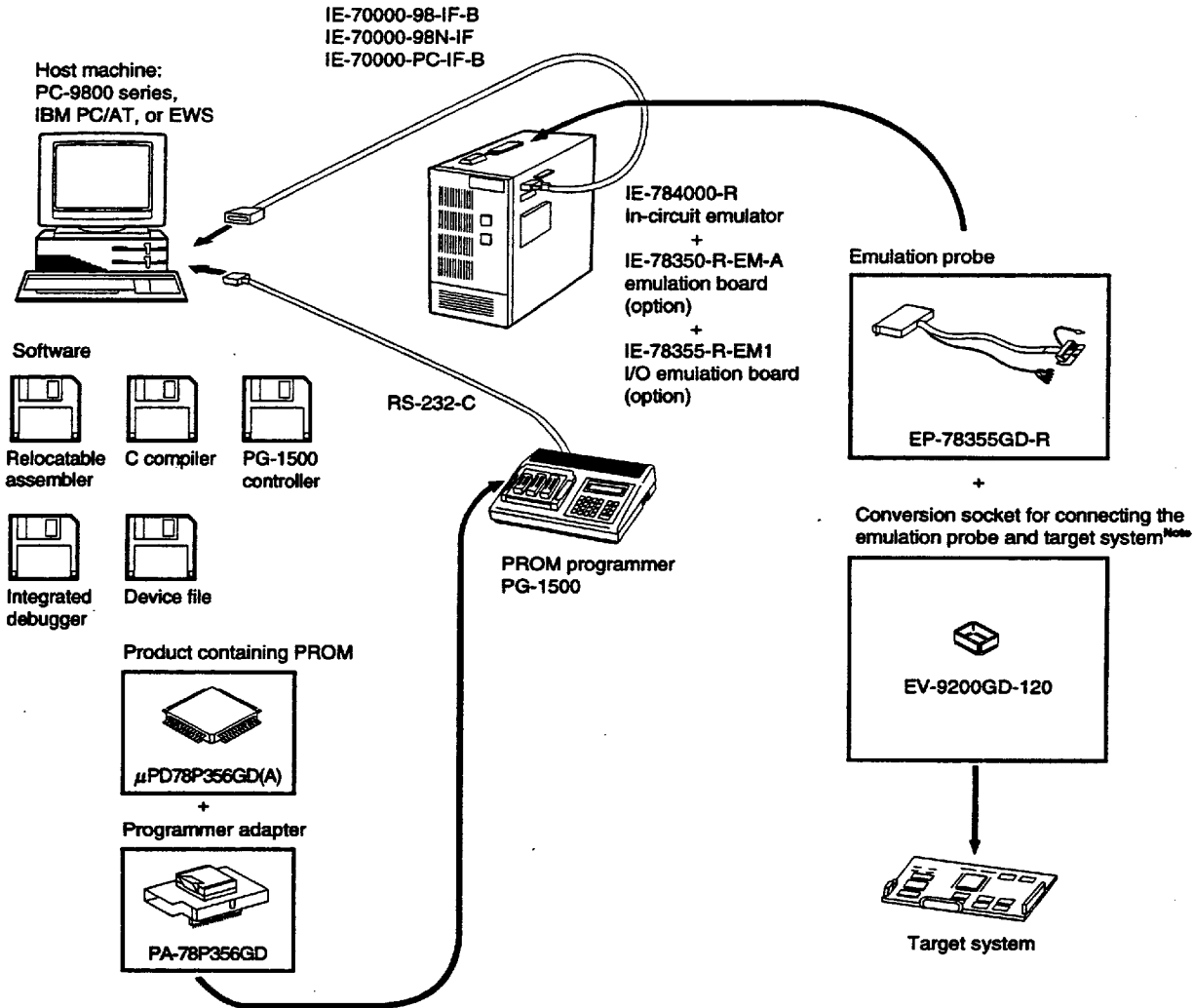
Hardware	IE-784000-R	In-circuit emulator for developing and debugging an application system. For debugging, connect the emulator to the host machine.			
	IE-78350-R-EM-A ^{Note}	Emulation board for emulating peripheral hardware such as the I/O ports of the target device.			
	IE-78355-R-EM1	I/O emulation board for emulating peripheral hardware such as the I/O ports of the target device.			
	EP-78355GD-R	Emulation probe for connecting the IE-784000-R to the target system. The EV-9200GD-120 conversion socket is supplied with the emulation probe, to connect the target system.			
	EV-9200GD-120				
	IE-70000-98-IF-B	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine.			
	IE-70000-98N-IF	Interface adapter and cable when a PC-9800 series notebook is used as the host machine.			
	IE-70000-PC-IF-B	Interface adapter when the IBM PC/AT is used as the host machine.			
IE-78000-R-SV3	Interface adapter and cable when the EWS is used as the host machine.				
Software	Integrated debugger (ID78K3)	Program for controlling the in-circuit emulator for the 78K/III series. The integrated debugger (ID78K3) is used together with the device file (DF78355). Debugging can be performed for the source program written in C, structured assembly language, or assembly language. The ID78K3 can display various information simultaneously on the host machine screen divided into multiple areas. This ensures efficient debugging.			
		Host machine		Part number	
		OS	Distribution media		
		PC-9800 series	MS-DOS + Windows™	3.5-inch 2HD	μSAA13ID78K3
				5.25-inch 2HD	μSAA10ID78K3
		IBM PC/AT or compatibles (Japanese Windows)	PC DOS + Windows	3.5-inch 2HC	μSAB13ID78K3
				5.25-inch 2HC	μSAB10ID78K3
		IBM PC/AT or compatibles (Windows)		3.5-inch 2HC	μSBB13ID78K3
				5.25-inch 2HC	μSBB10ID78K3
		Device file (DF78355) ^{Note}	File which contains the device-specific information. The device file (DF78355) is used together with the assembler (RA78K3), C compiler (CC78K3), or integrated debugger (ID78K3).		
	Host machine		Part number		
	OS			Distribution media	
	PC-9800 series		MS-DOS	3.5-inch 2HD	μS5A13DF78355
				5.25-inch 2HD	μS5A10DF78355
IBM PC/AT or compatibles	PC DOS		3.5-inch 2HC	μS7B13DF78355	
			5.25-inch 2HC	μS7B10DF78355	

Note Under development

Remark It is guaranteed that the integrated debugger and device file run only under the OSs on the corresponding host machines described above.

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Development tool configuration (when the integrated debugger is used)



Note The conversion socket is supplied with the emulation probe.

- Remarks** 1. In this figure, a 3.5-inch floppy disk is shown as an example distribution medium of software.
2. In this figure, a desk-top personal computer is shown as an example host machine.

A.2 EMBEDDED SOFTWARE

To improve the efficiency of program development and simplify the maintenance of systems incorporating this microcomputer, the following embedded software is provided.

Real-time OS

Real-time OS (RX78K/III) ^{Note}	This operating system was designed to provide a multitasking environment for control applications that require real-time processing. System performance is improved by using the idling CPU for other processing. RX78K/III provides system calls that conform to μTRON specifications. The RX78K/III package provides the RX78K/III nucleus and a tool (Configurator) that is used for creating multiple information tables.			
	Host machine	OS	Distribution media	
	PC-9800 series	MS-DOS	3.5-inch 2HD	Undecided
			5.25-inch 2HD	Undecided
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	Undecided
5.25-inch 2HC			Undecided	

Note Under development

Caution Before purchasing this software, complete the purchase application sheet and sign the software license agreement.

Remark To use the RX78K/III real-time operating system, the optional RA78K3 assembler package is required.

Fuzzy inference development support system

Tool for creating fuzzy knowledge data (FE9000, FE9200)	This program supports the input/editing and simulation of fuzzy knowledge data (fuzzy rules and membership functions).			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FE9000
			5.25-inch 2HD	μS5A10FE9000
	IBM PC/AT or compatibles	PC DOS + Windows	3.5-inch 2HC	μS7B13FE9200
5.25-inch 2HC			μS7B10FE9200	
Translator (FT78K3) ^{Note}	This program converts fuzzy knowledge data, obtained using the tool for creating fuzzy knowledge data, into an assembler source program for RA78K3.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FT78K3
			5.25-inch 2HD	μS5A10FT78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13FT78K3
5.25-inch 2HC			μS7B10FT78K3	
Fuzzy inference module (F178K/III) ^{Note}	This program performs fuzzy inference by linking the fuzzy knowledge data converted by Translator.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13F178K3
			5.25-inch 2HD	μS5A10F178K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13F178K3
5.25-inch 2HC			μS7B10F178K3	
Fuzzy inference debugger (FD78K/III)	This software supports the evaluation and adjustment of fuzzy knowledge data at the hardware level, by using an in-circuit emulator.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FD78K3
			5.25-inch 2HD	μS5A10FD78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13FD78K3
5.25-inch 2HC			μS7B10FD78K3	

Note Under development

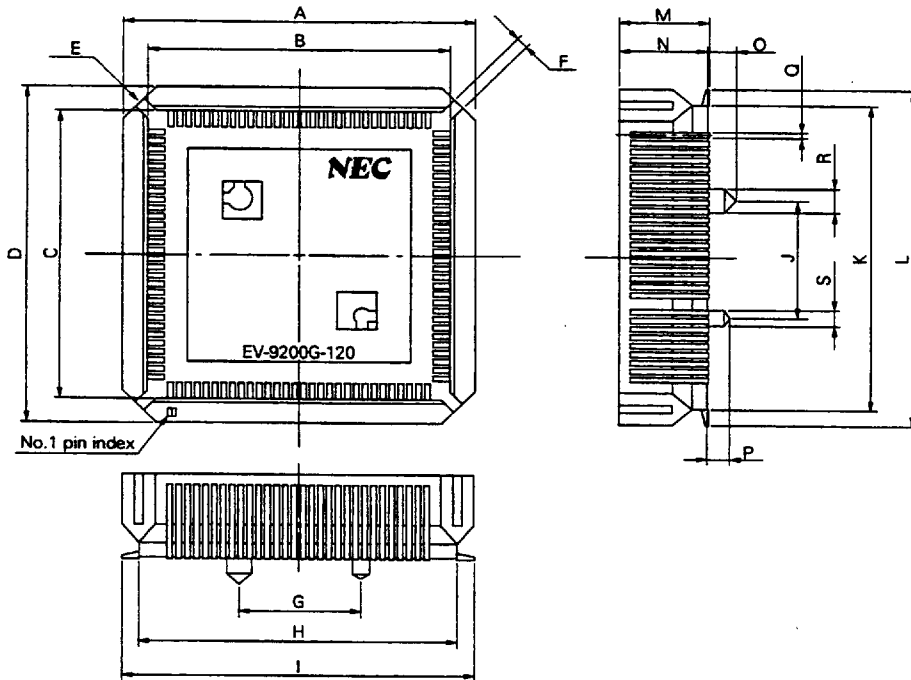
■ 6427525 0084737 660 ■

APPENDIX B DRAWINGS OF THE CONVERSION SOCKET AND RECOMMENDED PATTERN ON BOARDS

Caution Although the part number is EV-9200GD-120, number EV-9200G-120 is marked on the part.

Fig. B-1 Drawings of the Conversion Socket (EV-9200GD-120) (Reference)

Based on EV-9200G-120
(1) Package drawing (in mm)



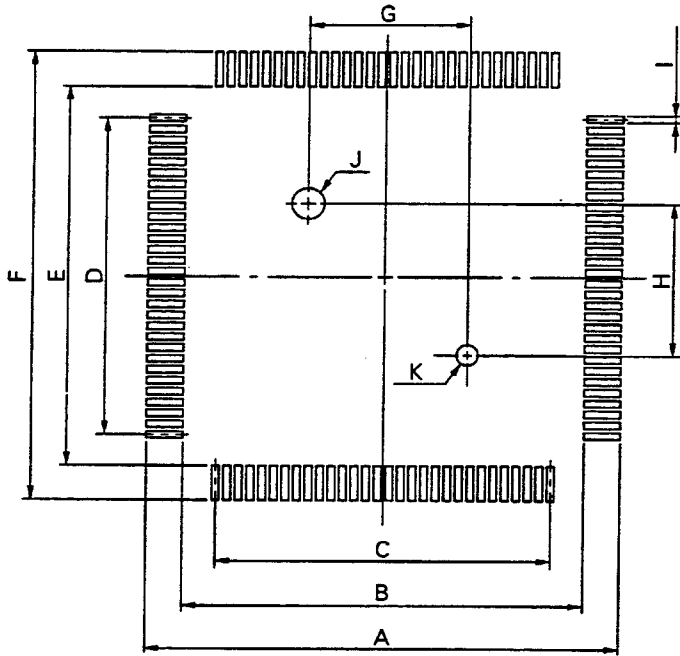
EV-9200G-120-G0

ITEM	MILLIMETERS	INCHES
A	32.3	1.272
B	27.6	1.087
C	27.6	1.087
D	32.3	1.272
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	11.0	0.433
H	29.3	1.154
I	32.0	1.26
J	11.0	0.433
K	29.3	1.154
L	32.0	1.26
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	0.35±0.1	0.014 ^{+0.004} _{-0.005}
R	φ2.3	φ0.091
S	φ1.5	φ0.059

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Fig. B-2 Recommended Pattern on Boards for the Conversion Socket (EV-9200GD-120)
(Reference)

Based on EV-9200G-120
(2) Pad drawing (in mm)



EV-9200G-120-P0

ITEM	MILLIMETERS	INCHES
A	$0.8 \pm 0.02 \times 29 = 23.2 \pm 0.05$	$0.031^{+0.002}_{-0.001} \times 1.142 = 0.913^{+0.003}_{-0.002}$
B	28.3	1.114
C	33.0	1.299
D	$0.8 \pm 0.02 \times 29 = 23.2 \pm 0.05$	$0.031^{+0.002}_{-0.001} \times 1.142 = 0.913^{+0.003}_{-0.002}$
E	28.3	1.114
F	33.0	1.299
G	11.0 ± 0.08	$0.433^{+0.004}_{-0.003}$
H	11 ± 0.08	$0.433^{+0.004}_{-0.003}$
I	0.5 ± 0.02	$0.02^{+0.001}_{-0.002}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Cautions on CMOS Devices**① Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged. Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② CMOS-specific handling of unused input pins

Caution Hold CMOS devices at a fixed input level. Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor. If handling of unused pins is documented, follow the instructions in the document.

③ Statuses of all MOS devices at initialization

Caution The initial status of a MOS device is unpredictable when power is turned on. Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined. When you turn on a device having a reset function, be sure to reset the device first.

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ITRON stands for Industrial TRON.